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TOTAL DOSE RESPONSE OF SILICON-ON-INSULATOR (SOI) METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR'S (MOSFET'S)

A Thesis Presented

by

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to

The Department of Electrical and Computer Engineering

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for the degree of

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ABSTRACT

Total dose response of both NMOS and PMOS FET's fabricated on SIMOX and ZMR substrates was studied. Two types of back channel leakage currents were identified for the SIMOX devices. A back channel leakage due to MOSFET action uses the substrate bias as the gate bias. The other component is due to soft reverse characteristics of the body-drain junction.

The back channel leakage due to MOSFET action varies with the substrate bias and thus varies with irradiation due to threshold voltage shift. The soft reverse current is a function of drain-body voltage and hence varies with substrate bias and irradiation. The threshold voltage, I-V characteristics, and subthreshold currents of both front and back channels as a function of total dose were obtained.

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TABLE OF CONTENTS

I. INTRODUCTION

1.1 Silicon-on-Insulator Transistors

Silicon-on-Insulator (SOI) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET's) differ from conventional bulk MOSFET's because there is a buried oxide in the silicon substrate just below the active device region (See Figure 1). This buried dielectric isolation gives SOI MOSFET's several advantages over bulk MOSFET's for various applications.

The first advantage is that the parasitic junction capacitances are reduced, which results in a higher speed of operation. Second, the built-in isolation results in freedom from latch-up. Third, the isolation area around devices is reduced, resulting in higher packing densities. Fourth, the buried isolation results in the possibility of three-dimensional circuits with even further increases in speed and decreases in volume. Finally, the small, isolated silicon volume of SOI devices results in increased tolerance to single particle and transient radiation upsets.

The increased tolerance or "hardness" to single particle and transient radiation of SOI devices makes them excellent candidates for nuclear and space radiation hardened electronics required for many military and space applications. However, like bulk MOSFET's, SOI MOSFET's still have the problem of threshold voltage shift due to positively charged ions trapped in the gate oxide and at the silicon-gate oxide interface after ionizing irradiation. In addition, SOI MOSFET's have a similar problem with the buried oxide at the back

channel which results in excess leakage currents. Further study of the SOI MOSFET operation as a function of radiation and resultant improvements in processing are necessary to make SOI MOS technology viable for nuclear and space radiation environments.

1.2 Silicon-on-Insulator Technologies

The early technologies which fit into the category of Silicon-on-Insulator are heteroepitaxial Silicon-on-Sapphire (SOS) and polysilicon substrate Dielectric Isolation (poly DI). They are still in use today, but SOS, in particular, has difficult material problems to overcome. Today, SOI generally means a single crystal silicon film on a silicon dioxide (or other insulating) layer on a single crystal silicon substrate.

Schott and Schedd (1986) recently reviewed the leading technologies for SOI devices. Separation by Implantation of Oxygen (SIMOX) uses a high current ion implanter to implant large doses of oxygen in silicon wafers, which results in silicon dioxide forming at the desired depth. Zone Melt Recrystallization (ZMR) typically uses a graphite strip heater to recrystallize polysilicon deposited on a thermally grown oxide. Full Isolation by Porous Oxidized Silicon (FIPOS) uses an electrochemical etch process to make the field areas and the material below the device active areas porous. The pores then allow rapid oxidation, resulting in a fully isolated silicon island. SIMOX and ZMR are the leading technologies for thin film MOS devices and are studied in this thesis. Other technologies such as Bond and Etchback are being developed but are

better suited to thick film bipolar devices and will not be studied here.

1.3 Nuclear and Space Radiation Fundamentals

In order to study the effects of nuclear and space radiation on SOI MOSFET's, the fundamentals of radiation must first be introduced. The various types of irradiating particles can be grouped into three major categories: photons (x-rays and gammas), neutrons, and charged particles (electrons, protons, alpha particles and heavy ions). Photons have zero rest mass. Photons and neutrons are charge neutral. Nuclear explosions generally give rise to pulses of gamma rays and neutrons, whereas the space environment consists of a low-level, constant flux of charged particles.

Although the interaction of radiation with materials can be complex, the effect on solid-state electronics can be limited to two major areas: ionization (electron-hole generation) and displacement damage (dislodging atoms from their normal lattice sites). In general, particles passing through electronic material give off energy which results in ionization and atomic displacement. This can be simplified even further in that the majority of a photon's or charged particle's energy is given off to ionization and the majority of a high-energy neutron's energy results in displacement damage [Mclean (1987)].

Before continuing, the terminology for radiation exposure needs to be mentioned. Neutron exposure of a sample is commonly given in terms of neutron fluence, n/cm^2, where particle fluence is the time integral

of the flux, and flux is in units of particles/cm^2-s. For photons and charged particles, the amount of energy that goes into ionization is a function of the stopping power of a given material. The commonly used unit of radiation absorbed into a given material is the rad (radiation absorbed dose).

The major nuclear radiation effect on SOI MOSFET's is due to gamma rays and is the only effect to be discussed further. Displacement damage from neutrons does not have a significant effect on the majority carrier MOSFET for digital applications, and upsets from prompt (fast initial rise-time) neutron fluence are minimized in the SOI structure.

1.4 Survey of Previous Research

Manasevit and Simpson (1964) developed the idea of SOS in 1963. By 1971 SOS wafers were commercially available, and by 1976 Hewlett Packard had developed a 16-bit microprocessor using SOS technology. In a review of SOS CMOS technology by Sato et al. (1984), the authors confirmed that SOS CMOS is 1.2 to 2.5 times faster than bulk CMOS and occupies about 30% less area, in addition to being latch-up free. However, the material mismatch between silicon and sapphire is difficult to overcome. Impurities are introduced into the silicon layer from sapphire films, the silicon crystal is imperfect due to the the mismatch of crystalline constants, and the thermal expansion difference of silicon and sapphire film causes large residual strain after cooling. These defects all result in reducing the mobility constant of the silicon. Each of today's SOI technologies has its own silicon crystal defect problems,

today's SOI technologies has its own silicon crystal defect problems, but due to the compatibility of silicon and silicon dioxide, these problems are not as troublesome as with SOS technology.

The rudimentary beginning of SIMOX technology was when Smith (1956) first proposed the synthesis of dielectric layers through ion implantation, but it was not until much later that Watanbe and Tooi (1966) demonstrated the technology. Obtaining low defect single crystal silicon above the implanted oxide remained a challenge until Izumi et al. (1978) reported fabricating MOS devices on oxygen implanted substrates. Since then, SIMOX technology has received much attention.

Hughes and Giroux (1964) conducted ionizing radiation experiments on MOSFET's that resulted in large changes in the transconductance of those devices. Szedon and Sandor (1965) were among the first to explain that those results were due to the formation of trapped positive charges in the gate oxide. This happens when ionizing irradiation generates electron-hole pairs. Many of the much more mobile electrons are swept away before recombination can occur, which results in holes being trapped in the oxide or at the $Si-SiO_2$ interface. The principal effect of the trapped charges is a negative shift in the threshold voltage. Since additional positive charges are now always present between the gate and the channel region, less voltage is necessary to turn on a device.

In SOI devices, holes are trapped in the buried oxide as well as in the gate oxide. The trapped holes in the buried insulator induce an unwanted back channel in n-channel MOSFET's that results in leakage

conditions and irradiation dose). Tsaur et al. (1982) reported that applying a moderate negative bias (-15V) to the substrate of an n-channel MOSFET during irradiation will reduce the negative threshold voltage shift and thus reduce the back-channel leakage current. In this case, the applied negative bias causes an electric field favorable to sweeping away more of the holes before they are trapped. Unfortunately, applying -15V to the substrate of a p-channel MOSFET turns on the parasitic back-channel. In order to show this technique is useful for CMOS circuits, Tsaur et al. (1984) demonstrated that a substrate bias during irradiation of -5V greatly decreases the total dose radiation sensitivity of n-channel devices without significantly impairing the operation of p-channel devices. However, Davis et al. (1985) showed that a back gate bias reduces the transient hardness of CMOS/SOI devices. So the effects of the back gate bias on transient upset should also be considered in order to optimize the circuit performance in a radiation environment.

Another way to negate the effects of radiation on the back channel is to heavily dope the channel near the buried oxide to raise the threshold voltage of the parasitic back channel. Thus the device will be immune to much larger total doses before the back channel begins to turn on. Mao et al. (1986) showed that the front gate of such a device behaves the same as a conventional bulk MOS device. Furthermore, a negative substrate bias, which reduces the voltage shift of the back channel, has no effect on the front channel. (This assumes the channel region is thick enough so that the front and back channels do not

region is thick enough so that the front and back channels do not interact with each other under typical bias conditions.) Mao et al. (1986) also observed a positive threshold voltage shift of the back channel for low doses (<100 krads) and negative substrate bias before the threshold voltage shift turned negative with increased dose. Heavily doping the back channel, however, is not without problems. Bahraman et al. (1988) notes that this results in a n^+p^+ drain-to-body diode, which has a low breakdown voltage and higher reverse saturation leakage current.

Another important leakage current in any MOSFET is the reverse saturation current of the drain-body p-n junction. A. Goetzberger and W. Shockley (1960) demonstrated "soft" or rounded reverse current characteristics in p-n junctions at voltage levels below avalanche breakdown due to metal precipitates in the silicon. P.L.F. Hemment (1979) showed that silicon samples were contaminated with high concentrations of metal impurities (as much as one percent of the primary dose) during ion implantation. R. Sundaresan et al. (1987) proposed that the physical mechanism causing high junction leakage currents in SIMOX SOI MOSFET's is electric field-enhanced emission of carriers through traps near the buried-oxide/silicon interface. These traps are a result of the metal impurities introduced during the oxygen ion implantation. They also reported that the leakage current was a strong function of drain voltage, substrate voltage and, to a lesser extent, front gate voltage. Finally, they noted that the leakage current increased with back channel doping.

in the negative threshold voltage shift with reduced buried oxide thickness and extended their research in 1988 to leakage currents, reporting a decrease in the leakage current by two orders of magnitude when the oxygen dose was reduced from 2.25×10^{18} to 1.4×10^{18} cm^2. Since they expected a linear decrease with oxygen dose, they studied the microstructure and found that the lower dose wafer had silicon inclusions in the buried oxide adjacent to the silicon film/buried oxide interface. They proposed that these silicon islands provide extra interfacial areas for impurity gettering, since metal impurities tend to segregate to this interface. Furthermore, since these gettering sites are away from the active device region, they may be very effective in reducing the junction leakage current, resulting in a much more than linear decrease in the leakage current with decreasing oxygen dose. The negative side effect of reducing the buried oxide thickness is increased buried oxide capacitance and must be considered when determining the optimum thickness.

Somewhat in contrast to Sundaresan's theory, L. Jastrzebski (1988) reported that the leakage current had a strong dependence on the carbon concentration, whereas the dependence on the heavy metal concentration was not as straightforward.

One primary difference in electrical characteristics between SOI MOSFET's and conventional bulk MOSFET's is a result of the floating body and is known as the kink effect. Channel carriers in an SOI MOSFET operating at high applied voltage generate electron-hole pairs by impact ionization near the drain region. The generated holes travel to the

source, lowering the potential barrier for electrons flowing from the source to the channel. This results in an abrupt increase or kink in the I_D-V_D characteristics which makes the device unsuitable for analog applications [Kato (1985)]. Colinge (1988) performed numerical simulations and performed confirmation experiments to show that thin film, fully depleted SOI MOSFET's do not exhibit the kink effect. This is due to the reduction of the drain electric field, bringing about a lower impact ionization probability, and due to the reduced substrate-to-source potential barrier which prevents accumulation of holes in the substrate. Furthermore, if a negative substrate bias is applied, the conditions for existence of a kink reappear. Mao et al. (1988) report that the floating body effect is more pronounced in lower oxygen dose substrates. This is a result of the reduced junction leakage which causes a higher body node potential under the same biasing conditions.

The subthreshold slope is an important parameter of MOSFET's as it is a measure of how fast a transistor turns on and off, governing the potential speed of a circuit. It is expressed as the change in the gate voltage required to reduce the drain current by an order of magnitude. Davis et al. (1986) reported SOI MOS n-channel transistors which exhibited the kink effect had abnormally high subthreshold slopes. They observed decreases in the slope with increasing drain voltage and decreasing channel length. Fossum et al. (1987) obtained similar results and derived equations which explain the steeper slope and observed dependences on drain voltage, channel length and leakage current in terms of the floating-body charging due to carrier generation

at the drain, including the channel current-induced impact ionization.

It is now clear that there are various mechanisms contributing to what is commonly lumped together in the term leakage current. However, no one has separated the leakage current into its components. This study will characterize SOI MOSFET's as a function of total dose, concentrating on identifying the various leakage current components.

II. EXPERIMENTAL

2.1 Description of SOI MOSFET's Studied

Various NMOS and PMOS FET's fabricated on SOI substrates were studied. Both SIMOX and ZMR technologies were included. These devices have various channel lengths, geometries, buried oxide thicknesses, and silicon overlay thicknesses, both with and without an epi layer. The particulars of these devices are shown in Table I. Types A, B, C and D indicate the different research groups who supplied the devices for this study. Both n- and p-channel MOSFET's were studied for each channel length listed unless only one type is indicated. The National Bureau of Standards's (NBS) structure is shown in Figure 1, the enclosed gate structure is shown in Figure 2, the H gate structure is shown in Figure 3, and the round gate structure is shown in Figure 4. The enclosed gate FET's do not have leakage currents along the edge of the channel inherent in the NBS structure. The H gate and round gate structures have a body contact made via a p^+ region adjacent to the p body or channel region. The SIMOX devices are CERDIP packaged devices. The ZMR devices are on a wafer. The research organizations which provided the devices considered the doping particulars of the source, body and drain regions to be proprietary and, therefore, did not provide such information.

TABLE I

Fabrication Details of the Silicon-on-Insulator MOSFET's

	TYPE A	TYPE B	TYPE C	TYPE D
Technology	SIMOX	SIMOX	SIMOX	ZMR
W/L (um), Structure	25/5, NBS	31.2/3.6, enclosed	30/5, H, n-chan	45/3, H
	25/2, NBS	31.2/1.2, enclosed	10/5, H, p-chan	
	25/1.25, NBS	7.2/1.2, H	--/5, round,n-chan	
Gate Oxide (nm)	35	25	25-30	36.5
Buried Oxide				
Thickness (nm)	380	330-350	440	1,000
O_2 Dose ($/cm^2$)	1.5×10^{18}	1.4×10^{18}	1.9×10^{18}	NA
Anneal T (^oC)	1300, 1325, 1375	1275	1250-1300	NA
Anneal Time (hrs)	1.5	4-10	4-6	NA
Company	Eaton		Eaton/Spire	NA
Channel Region				
Si Thickness (nm)	200	280	400-600	300
Epi Layer	No	Yes	Yes	Yes

2.2 Test Facilities and Equipment

Gamma total dose radiation testing of the SIMOX devices was carried out in the Cobalt^{60} radiation chamber located at Rome Air Development Center, Hanscom AFB, MA. The ZMR devices were tested in an Aracor 4100XP x-ray system. It was convenient to test the ZMR devices on the Aracor system because they are on a wafer.

All data was taken with a Hewlett Packard HP4145B Semiconductor Parameter Analyzer and a HP16058A Test Fixture. The current resolution of this equipment combination is $\pm$1 pA. In the case of the ZMR wafer, however, the wafer was left in the x-ray machine during data measurements and the HP 16058A was only used as a connection board for wires from the wafer probe card to the HP 4145B. In this case, more noise was present and the current resolution was approximately $\pm$50 pA.

2.3 Procedure

Prior to irradiation, various I-V characteristics and leakage currents of each device were obtained using the HP4145B. The devices were treated as two-gated MOSFET's. A typical structure is shown in Figure 5. The front gate voltage is V_G, the back gate (substrate) voltage is V_{G1}, the body voltage is V_B, the drain voltage is V_D and the source voltage is V_S.

The drain, source, front gate and back gate currents were all monitored as a function of V_D and V_G for both the front and back channels. The front channel data was obtained by applying the proper bias to the back gate to turn the back channel off, and the back channel

data was obtained by applying the proper bias to the front gate to turn the front channel off.

In addition to these measurements, more tests were performed on the devices with a body contact. The drain-body and source-body junction leakage currents were obtained as a function of body voltage with the front and back channels turned off. These devices were also operated as a bipolar junction transistor by varying the body and drain voltages and monitoring the body, source, drain and back gate currents.

During irradiation, the Type B and some Type A devices were left floating. The remaining Type A devices as well as the Type C and Type D devices had a -5V substrate bias and a +5V front gate bias during irradiation. Also, the n-channel devices' source and drain were common while the p-channel devices' source was at +5V and its drain was common.

All the pre-radiation measurements were repeated after total accumulated doses of 50k, 100k, 200k, 500k and 1,000k rads(Si). All measurements were completed within 30 minutes after each irradiation step.

III. RESULTS

3.1 Threshold Voltage

The most prominent effect of gamma total dose radiation on a SOI MOSFET is the negative threshold voltage shift of both the front channel and the parasitic back channel (See sections 1.1 and 1.4). The threshold voltage of an ideal bulk MOSFET is calculated from the equation for drain current as shown in Sze (1985).

For the device operation in the linear region (V_D = 0.1 V):

$$I_D = Zu_nC_o(V_G - V_T)V_D/L \qquad \text{for } V_D << (V_G - V_T)$$

In this case, V_T is found by extrapolating the slope of an I_D-V_G curve to I_D=0V as shown in Figure 6.

For the device operating in the saturation region (V_D = 3 V):

$$I_{DSAT} = Zu_nC_i(V_G - V_T)^2/2L$$

In this case, V_T is found by extrapolating the slope of the SQRT(I_D)-V_G curve to SQRT(I_D)=0V as shown in Figure 7. These equations can be applied to both the front and back channels of a SOI MOSFET. Although these ideal equations may not give the most accurate absolute V_T possible, they will give a good relative value as a function of total dose.

The threshold voltage for various devices as a function of total dose can be seen in Tables II through V. Figures 8.A and 8.B compare the change in the threshold voltage for the different devices. Tables II.A and II.B show the threshold voltages for Type A n-channel and p-channel devices, respectively. Tables III and IV show the threshold

voltages for a Type B and a Type C n-channel device, respectively. Table V shows the threshold voltages for a Type D, ZMR, n-channel device. Due to the variety of unknown processing differences of the various device types, it is difficult to make comparisons of the total voltage shift between types for the 1000 krads(Si) dose.

Table II.A

Threshold Voltage as a Function of Total Dose

SIMOX SOI MOSFET, Type A, n-channel, NBS

V_T[1]

krads	FRONT GATE 5 um	FRONT GATE 2 um	FRONT GATE 1.25 um	BACK GATE 5 um	BACK GATE 2 um	BACK GATE 1.25 um
0	0.54	0.53	0.44	8.51	8.11	7.78
50	0.073	-0.205	-0.246	5.64	3.53	3.47
100	-0.066	-0.263	-0.266	4.47	3.31	3.29
200	-0.387	-1.34	-1.36	1.99	-3.05	-2.94
500	-1.05	-2	-1.85	-0.914	-12.09	-12.22
1000	-1.56	-2	-1.9	-2.05	-19.79	-19.98

[1]Extrapolation of I_D, V_{DS}=0.1V
V_{G1}=-5V during irradiation

Table II.B

Threshold Voltage as a Function of Total Dose

SIMOX SOI MOSFET, Type A, p-channel, NBS

V_T [1]

	FRONT GATE			BACK GATE		
krads	5 um	2 um	1.25 um	5 um	2 um	1.25 um
0	0.359	0.463	0.613	-5.16	-5.24	-4.78
50	-0.052	0.034	0.141	-7.43	-7.58	-7.07
100	-0.202	-0.155	-0.049	-8.16	-8.35	-7.86
200	-0.365	-0.383	-0.284	-9.18	-9.27	-8.85
500	-0.579	-1.05	-0.926	-10.7	-12.4	-11.5
1000	-0.781	-1.72	-1.60	-11.85	-15.5	-14.36

[1]Extrapolation of I_D, V_{DS}=-0.1V
V_{G1}=-5V during irradiation

Table III

Threshold Voltage as a Function of Total Dose

SIMOX SOI MOSFET, Type B, n-channel, H gate

V_T[1]

	FRONT GATE			BACK GATE		
krads	3.6 um*	1.2 um*	1.2 um#	3.6 um*	1.2 um*	1.2 um#
0	0.48	0.44	0.49	18	19.4	15.8
100	0.45	0.43	0.49	9.7	10.3	12.8
500	0.4	0.41	0.47	-0.3	0.5	0.14
1000	0.40	0.42	---	-3.2	-2.5	---

*Enclosed gate #H gate
[1]Extrapolation of SQRT(I_D), V_{DS}=5V
V_{G1}=0V during irradiation

Table IV

Threshold Voltage as a Function of Total Dose

SIMOX SOI MOSFET, Type C, n-channel, Round

	V_T[1]	
	FRONT GATE	BACK GATE
krads	5 um	5 um
0	0.115	11.12
50	-0.022	7.11
100	-0.154	6.63
200	-0.424	5.79
500	-1.17	3.89
1000	-2.09	2.35

[1]Extrapolation of I_D, V_{DS}=0.1V
V_{G1}=-5V during irradiation

Table V

Threshold Voltage as a Function of Total Dose

ZMR SOI MOSFET, Type D, n-channel, H gate

	V_T	
	FRONT GATE[1]	BACK GATE[2]
krads	3 um	3 um
0	1.22	23.1
100	0.592	~25
500	-1.86	19.9
1000	-3.69	15.6

[1]Extrapolation of I_D, V_{DS}=0.1V
[2]Extrapolation of SQRT(I_D), V_{DS}=3V
V_{G1}=-5V during irradiation

However, the quality of the front and buried oxides differ enough between SIMOX and ZMR devices so that a comparison can be made between them. Figure 8.A shows that the front gate of the ZMR device (Type D) has a significantly larger threshold voltage shift than the three SIMOX devices. The reason postulated for the larger negative V_T shift of the front channel is due to the larger amount of interface traps which are present at the gate oxide-silicon interface in the ZMR device. Since zone-melt recrystallizing silicon deposited using chemical vapor deposition or similar technique does not result in a surface as smooth as a highly polished wafer, growing a thermal oxide on this rough surface results in more interface traps being formed. Additional interface traps means more charges are trapped during radiation and thus a larger V_T shift.

Similarly, the back gate interface between the wafer and thermally grown buried oxide of the ZMR device should have less interface traps than the ion implanted buried oxide-silicon interface of the SOI device. Figure 8.B shows that the threshold voltage shift of the back gate of the ZMR (Type D) device is smaller than the three SIMOX devices, but the small difference, coupled with a small sample size, is not conclusive evidence that the ZMR back gate threshold shift is much less than the SIMOX devices. Due to other competing factors, such as the much thicker buried oxide of the ZMR device which would result in additional oxide trapped charges, and various back channel dopings in the SIMOX devices, the effect of the increased inherent back channel hardness of the ZMR device is masked.

3.2 SIMOX Substrate MOSFET I-V Characteristics

The I_D-V_D characteristics of the front channel of an n-channel MOSFET, with the back channel turned off by applying a -5V bias on the back gate, is shown in Figure 9.A. The back channel I_D-V_D characteristics of the same device, with the front channel turned off by applying a -5V bias on the front gate, is shown in Figure 9.B. This is a Type A device (Refer to Table I). From the plots it is clear that a -5V bias on the front gate turns the front channel off and a -5V bias on the back gate turns the back channel off. Back channel transistor characteristics are not as normal as those the front channel. After subjecting this device to a total dose irradiation of 1 Mrad(Si), the front channel and back channel I_D-V_D characteristics were obtained and are shown in Figure 10. The front channel characteristics after 1 Mrad(Si) total dose are shown in Figure 10.A when the bias on the back channel is -5V. Similar characteristics for a back channel are shown in Figure 10.B. The threshold voltage shift is approximately -2V for the front channel and approximately -10V for the back channel (See Table II.A); thus there is a back channel current at V_{G1}=-5V (See Figure 10.B). Because front channel currents were measured at V_{G1}=-5V, the back channel contribution is included in them. Actually the back gate bias should have been even below -5V, perhaps -6V or -8V, to obtain only the front channel currents.

3.3 SIMOX Substrate MOSFET Subthreshold Characteristics

The subthreshold characteristics of both the front channel (with back channel off) and the back channel (with front channel off) of an n-channel device are shown in Figures 11.A and 11.B, respectively. This is a Type B, H gate device (Refer to Table I). The characteristic curves shown are for pre-radiation, 100k and 500k rads(Si) cases. The front channel characteristics show no shift in the threshold voltage from pre-rad to 500k rads(Si). The front channel current at V_G=-5V is really the back channel leakage current for every radiation dose. This can be understood by looking at Figure 11.B. This is the current we see in the front channel characteristics at V_G=-5V for the same radiation dose. The back channel characteristics show a considerable shift in the threshold voltage. The back channel characteristics also include the edge leakage component. We note that the current in accumulation increases and I_D increases with substrate bias and radiation dose. This is due to soft reverse junction characteristics at the back channel. This conclusion has been arrived at from additional test results and is discussed later.

The subthreshold characteristics of a p-channel device as a function of total dose are shown in Figure 12.A for the front channel and in Figure 12.B for the back channel. This is also a Type B, H gate device. There is no threshold voltage shift in the front channel as a function of total dose. There is a considerable shift in the threshold voltage of the back channel (Figure 12.B). Further, one sees a large increase in I_D in the front channel characteristics with an increase in

the total dose. This increased I_D is really back channel leakage current, as will be shown shortly. Back channel characteristics exhibit an increase in I_D with an increase in the radiation dose. The increase in I_D is due to the soft reverse junction characteristics. The soft reverse junction current increases with the increase in the reverse bias. The shift in the threshold voltage is in such a direction as to increase the reverse bias on the body-drain junction of a p-channel device. This V_T shift has a reverse effect on the body-drain junction of an n-channel device, and hence I_D decreases with the increase in total dose. The value of I_D determined at V_{G1}=3V and at a particular irradiation dose in the back channel characteristics is the value of I_D at V_G=3V and at that particular irradiation dose in the front channel characteristics (Figure 12).

As a point of interest, if the back gate is kept at 0V, the front channel leakage will reflect the back channel values seen at V_{G1}=0 in Figure 12.B. In this case, one sees that the leakage at pre-radiation falls between the 500k and 100k rads(Si) cases, unlike the case where V_{G1}=3V (Figure 12), where the leakage current increases with the radiation dose.

3.4 SIMOX Substrate MOSFET Junction Characteristics

In order to verify the soft reverse junction characteristics of the drain-body or source-body junctions, junction current as a function of bias (from -4V to +1V) was measured in an n-channel device which had a body contact (See Figures 3 and 5). The diode characteristics of both

drain- and source-body junctions, with both gates biased at -5V (both are off), are shown in Figure 13. The soft reverse characteristics are evident for both drain-body and source-body junctions, and the junctions are also seen to be more or less similar and symmetrical in shape. The drain-body characteristics as a function of bias for various substrate biases are also shown in Figure 13. The soft reverse biased drain leakage increases with an increase in the substrate bias. I_D is large for the same V_B (Figure 13) for V_{G1}=-10V compared to the case for V_{G1}=-5V and for V_{G1}=0V.

The drain-body characteristics as a function of front gate bias were also obtained. V_G was varied from 0 to -5V, and no discernible difference in I_D was noticed. From Table I we see that the buried oxide is at least 13 times thicker than the front gate oxide. Thus, the -20V applied to the back gate results in less E-field at the back channel than -5V applied to the front gate results in at the front channel; yet the drain leakage current increases with back gate bias but not with front gate bias. Hence, it is concluded that the leakage current is through the back channel and not through the front channel.

3.5 SIMOX Substrate Enclosed Gate Subthreshold Characteristics

To show that the soft characteristics are not due to the edge leakage, an enclosed gate Type B MOSFET was tested, and the results for an n-channel device are shown in Figure 14. The front channel characteristics are shown as a function of total dose in Figure 14.A and the back channel characteristics are shown in Figure 14.B. The front

channel does not show any shift in the threshold voltage, and when the device is biased into accumulation, the current seen is constant and is really due to the back channel leakage. The threshold shift for the back channel is very large, and in accumulation the device exhibits soft reverse junction characteristics. Due to the negative shift in the threshold voltage, the reverse soft junction characteristic current is less at increased total dose, and this back channel current at V_{G1}=-20V (Figure 14.B) is the magnitude of the current we see in the front channel at V_G=-5V (Figure 14.A). Similar characteristics for an enclosed gate p-channel device are shown in Figure 15.A for the front channel and in Figure 15.B for the back channel. The observations are similar to Figure 12. The characteristics in Figure 15 are smooth and somewhat uniformly shifted as a function of total dose compared to Figure 12. The characteristics in Figure 12 include edge leakage, and those in Figure 15 do not include edge leakage. It is interesting to observe that the soft reverse characteristics of the junction increase the back channel leakage of the p-channel and decrease the back channel leakage of the n-channel with an increase in the total dose.

Additional confirmation of the soft characteristics of an enclosed gate SIMOX substrate MOSFET is given in Figure 16. This is a Type C device. In Figure 16.B there is a significant reverse bias soft characteristic similar to that shown in Figures 11.B and 14.B.

3.6 ZMR Substrate MOSFET Characteristics

Subthreshold characteristics as a function of total dose of an n-channel ZMR MOSFET are shown in Figure 17. The front channel

characteristics are shown in Figure 17.A and those of the back channel in Figure 17.B. This is a Type D device (Refer to Table I). As discussed in section 3.1, Figure 17 confirms that the threshold voltage shift as a function of total dose is large for the front channel and relatively small for the back channel. More importantly, the back channel I_D does not increase with stronger accumulation (more negative back gate voltage), indicating that the soft reverse characteristics are not exhibited in ZMR MOSFET's. This observation is important for the conclusions that will be drawn at the end. The larger noise in Figure 17 is explained in section 2.2.

The I-V characteristics of the body-source and body-drain junction diodes of an n-channel ZMR SOI MOSFET with body contact are shown in Figure 18. Notice that both gates are biased into accumulation. In this case the soft reverse junction characteristics are not seen.

3.7 Additional Body Measurements

Another set of tests making contact to the body (p) region of the Type B, H-gate, n-channel device was conducted at pre-rad. In these tests V_{BS} was varied from -0.6V to +0.6V. The I_D-V_{DS}, I_B-V_{DS} and I_S-V_{DS} characteristics were obtained. The I_D-V_{DS} characteristics for various values of V_{BS} are shown in Figure 19.A. Similar I_B characteristics for various values of V_{BS} are shown in Figure 19.B, and I_S-V_{DS} characteristics for various values of V_{DS} are shown in Figure 19.C. The I_D-V_{DS} characteristics for V_{BS}=-0.6V to V_{BS}=+0.4V are similar, and for V_{BS}=+0.6V are different from the rest. The plot corresponds to a front

gate bias of -3V and a back gate bias of -15V (both channels are off). I_D is zero for a certain value of V_{DS} and starts increasing with an increase in V_{DS} (reverse bias). The increase in I_D is due to soft reverse junction characteristics. The reverse bias increases with a large value of $-V_{BS}$, and hence I_D increases with an increase in $-V_{BS}$ (Figure 19.A). The variation of I_B for V_{BS}=-0.6V to +0.4V is the mirror reflection of I_D. The current flows from drain to body. The device acts as a reverse biased p-n (body-drain) junction diode. The n-p (source-body) junction is also reverse biased, but the maximum magnitude of its reverse bias is only 0.6V and hence I_S is negligibly low compared to the drain and body leakage. The drain-body reverse junction leakage is high, due to the increased reverse bias (=V_{DS}-V_{BS}).

Now let us look at the I-V characteristic for V_{BS}=0.6V in Figure 19. There is a sharp transition in the value of all currents at V_{DS}=0V. V_{BS}=0.6V is the cut-in voltage of the junction. When V_{BS}=V_{BD}=0.6V (V_{BD}=0.6V at V_{DS}=0V), both body-drain and source-drain junctions are forward biased. Hence both drain and source leads drain the current from the body. The less the difference between I_D and I_S at V_D=0V for V_{BS}=0.6V, the greater the symmetry between the body-source and body-drain junctions. When V_{DS} is increased, V_{BD} drops below the cut-in voltage, and subsequently the body-drain junction becomes reverse biased. The source-body junction is always forward biased for V_{BS}=0.6V. The bias on the source (emitter) - body (base) junction is a forward bias, the bias on the body (base) - drain (collector) junction is a reverse bias, and the device operates as a bipolar junction transistor

with a small gain. The value of I_S (emitter current) is equal to the collector (drain) plus the base (body) currents. The device has a very poor h_{FE}. The increase in V_D and a corresponding decrease in I_B at high values of V_D are due to the soft characteristics, as shown in Figures 19.A and 19.B. It was also observed that when the bias on the back gate was less negative, the soft characteristics were less pronounced. This observation was made as a result of an experiment similar to the one described in Figure 19, except that V_{G1}=0V instead of V_{G1}=-15V. V_G=-3V in both cases. It is also interesting to note that I_S does not show these soft characteristics because the body-source junction is forward biased.

The above test of varying V_{BS} and measuring various currents (I_D, I_B and I_S) was performed as a function of total dose. The results of this test are shown in Figure 20. The I_D-V_{DS} characteristics for V_{BS}=0.6V as a function of total dose are shown in Figure 20.A. The I_B-V_{DS} characteristics as a function of total dose for V_{BS}=0.6V are shown in Figure 20.B, and the I_S-V_{DS} characteristics are shown in Figure 20.C. At V_{BS}=0.6V the device acts as a bipolar junction transistor except for the initial point at V_{DS}=0V, as we discussed in the case of Figure 19. The emitter (source) current = collector (drain) current + base (body) current, as seen in Figure 20. The soft reverse junction characteristics are seen in the drain current (Figure 20.A) and in the body current (Figure 20.B) at high values of reverse bias (+V_{DS}). The body and the source currents increase with an increase in total dose. The drain current increases with total dose of 100 krads(Si) but

decreases with further dose increase. This may be due to h_{FE} variation.

The I_D-V_{DS} characteristics of an n-channel device (discussed in Figures 19 and 20) as a function of total dose at V_{BS}=-0.6V are shown in Figure 21. At V_{BS}=-0.6V, the source-body and body-drain junctions are reverse biased for $+V_{DS}$. Both the front gate and back gate are biased into accumulation (V_G=-3V, V_{G1}=-15V). The current flowing through the body-drain junction is higher than the source-body junction due to increased reverse bias on the drain-body junction ($V_{DB}=V_{DS}-V_{BS}$), and hence $I_D=-I_B$ and $I_S<<I_D$. The drain current decreases while the total dose increases. The total dose induced positive charges in the oxide nullifies the effect of negative substrate bias. The accumulation potential required at the substrate at a certain dose is more negative than the pre-rad case. In effect the body-drain junction reverse bias decreases with the total dose, and therefore I_D decreases.

IV. DISCUSSION

Soft reverse junction characteristics were seen in SIMOX devices and not in the case of ZMR devices. These soft reverse junction characteristics at the back channel are due to metal contaminants in this channel. During oxygen implantation, metal contaminants in the ion beam path get embedded into the SIMOX substrate, and during annealing the metal contaminants get segregated at the back channel. The metal precipitates give rise to soft diode characteristics in the reverse bias mode of operation; a phenomenon which has been known for some time (See section 1.4).

The reverse soft characteristics due to metal precipitates in the back channel give rise to a back channel leakage current. This leakage is a function of the reverse bias on the body-drain junction. The magnitude of the reverse bias is affected by the back gate bias, the total dose, and the body potential. A certain back gate bias brings the device just into accumulation, and this voltage corresponds to the origin for the reverse characteristics of the junction. Radiation dose shifts the threshold voltage of the device, and this in effect results in shifting the point at which accumulation just starts and the origin of the reverse characteristics.

Another effect of total dose and change in back gate bias is the change in the carrier concentrations of the various transistor regions. By applying a bias on the substrate or by the radiation-induced trapped charges in the buried oxide, the carrier concentration in the drain

(n^+), source (n^+), body (p) and body contact (p^+) regions are affected (See Figure 1). When a bias is applied to accumulate the body region from p to p^+, the drain, source and body contact concentrations go from n^+ to n, n^+ to n, and p^+ to p^{++}, respectively. The variations depend upon the relative concentrations of every region. Therefore, there are various p-n junctions with concentrations that are continuously varied with the substrate bias and the radiation total dose.

Sze (1985) shows that

$$J_s = qD_p p_{no}/L_p + qD_n n_{po}/L_n$$

where J_s is the reverse saturation current density of the junction diode, and the other symbols have their usual meanings. The doping concentrations of both p-n (body-drain) regions are altered by the substrate bias and the radiation dose through MOSFET action. Therefore p_{no} and n_{po} change, causing J_s to change also. The doping concentration decreases in the p (body) and increases in the n (drain) due to radiation dose. The net change in J_s is small and depends upon the doping concentrations and doping profile of various regions. Therefore, the large reverse soft current characteristic is attributed to the metal precipitates in the back channel.

This soft reverse current due to the metal precipitates in the back channel is one of the leakage components of the back channel. The other component of back channel leakage is due to the MOSFET action with the substrate as the back gate. When a device is subjected to total dose radiation, the MOSFET action back channel leakage is affected more in the n-channel than in the p-channel due to negative threshold voltage

shift. The soft reverse leakage is affected more in the p-channel than in the n-channel due to the negative threshold shift. The negative threshold voltage shift increases the reverse bias on the body-drain junction of the p-channel device, thereby increasing the leakage current. The negative threshold shift decreases the reverse bias on the body-drain junction of the n-channel device, thereby decreasing the leakage current.

The separation of the two back channel leakage currents is shown in Figure 22. The I_D-V_{G1} plots for a p-channel device at pre-rad and 500 krads(Si) total dose are shown in the Figure. The back channel leakage due to MOSFET action is marked as Z in the Figure. This current due to MOSFET action current decreases from $6X10^{-4}$ to 10^{-11} A. The soft reverse junction current at pre-rad is marked as X_1 in the Figure. This leakage current increases from ~7 pA at the threshold voltage to 11 pA at V_{G1}=10V. The increased soft reverse leakage current due to irradiation is labeled as Y in the Figure. The leakage current increases considerably from ~8pA at pre-rad to ~6nA at 500 krads(Si). The total soft reverse junction current at 500 krads(Si) is then $X_2=X_1+Y$.

V. CONCLUSIONS

Two leakage current components of MOSFET's fabricated on SIMOX substrates have been identified. The back channel leakage normally referred to is due to MOSFET action with the substrate as the gate. This component increases in an n-channel device when it is irradiated due to the negative threshold voltage shift. The other component, the soft reverse leakage current, came to light by various experiments in this study. The soft reverse current characteristics are caused by the metal precipitates along the back channel. The soft reverse leakage current increases in a p-channel device when it is irradiated due to the negative threshold voltage shift.

It is evident from this study that the metal contaminants in the back channel have to be eliminated. The oxygen ion implantation process needs improvement to reduce the metal contaminants. Further, the ion implantation system design itself needs improvement as well to reduce the metal contaminants. The influence of these contaminants on electrical characteristics is very pronounced as evidenced by the experiments which were performed. In particular, irradiation enhances the effect of the metal contaminants in a p-channel device due to the negative threshold voltage shift as discussed above.

The MOSFET's fabricated on a ZMR substrate did not exhibit the soft reverse leakage current component which was shown to be characteristic of SIMOX devices. However, the poorer quality front gate oxide of the ZMR devices resulted in a much larger threshold voltage shift due to

irradiation. Thus the ZMR process needs to be improved to yield a better quality front gate oxide-silicon interface, which would reduce the number of interface traps and lessen the effect of irradiation.

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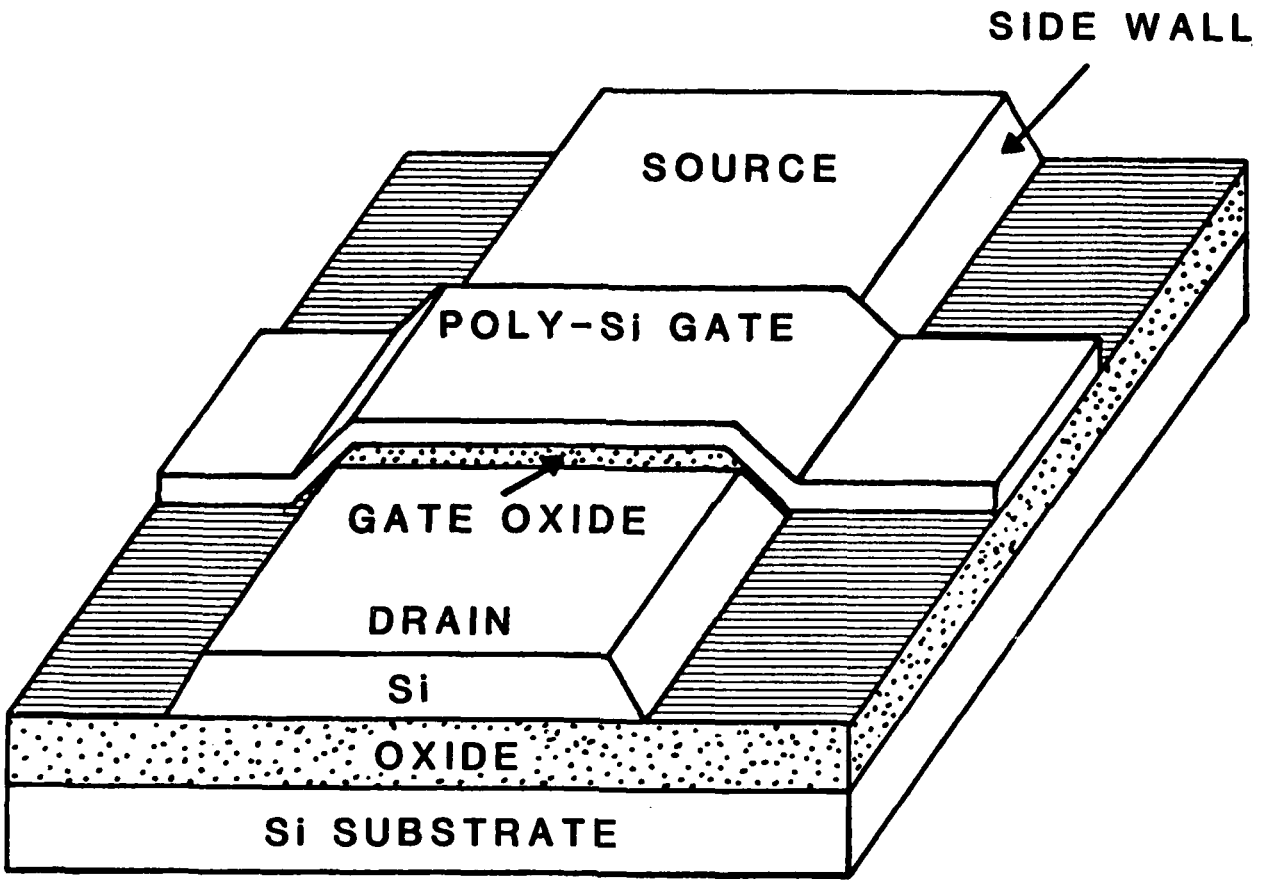


Figure 1. SOI MOSFET, NBS Structure

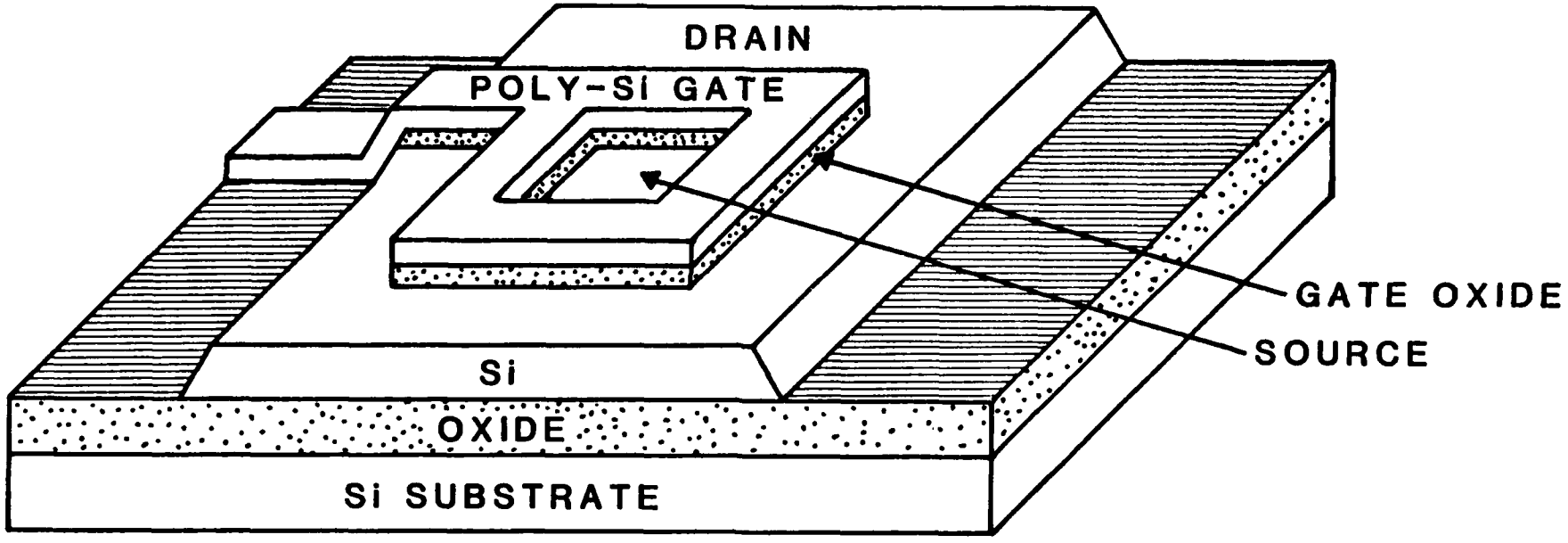


Figure 2. SOI MOSFET, Enclosed Gate Structure

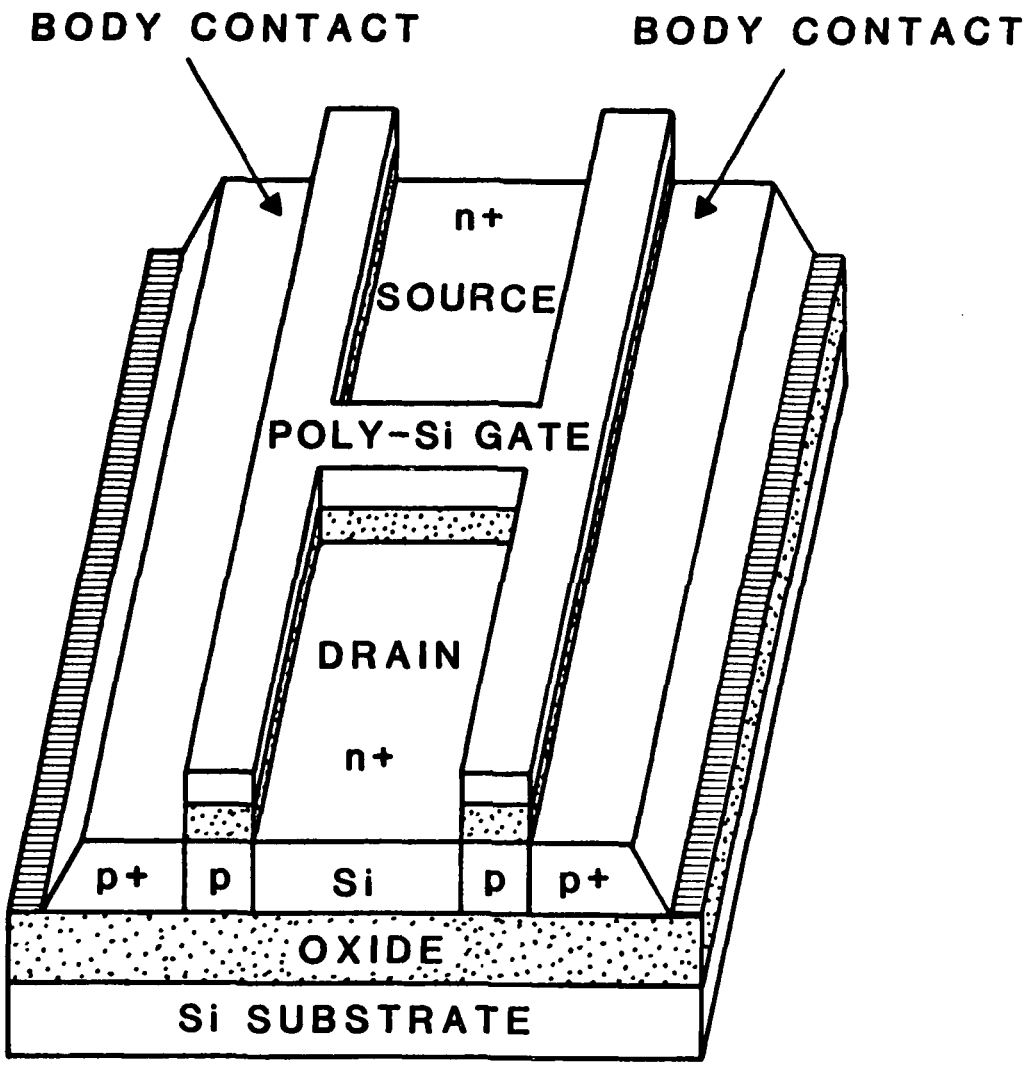


Figure 3. SOI MOSFET, H Gate Structure

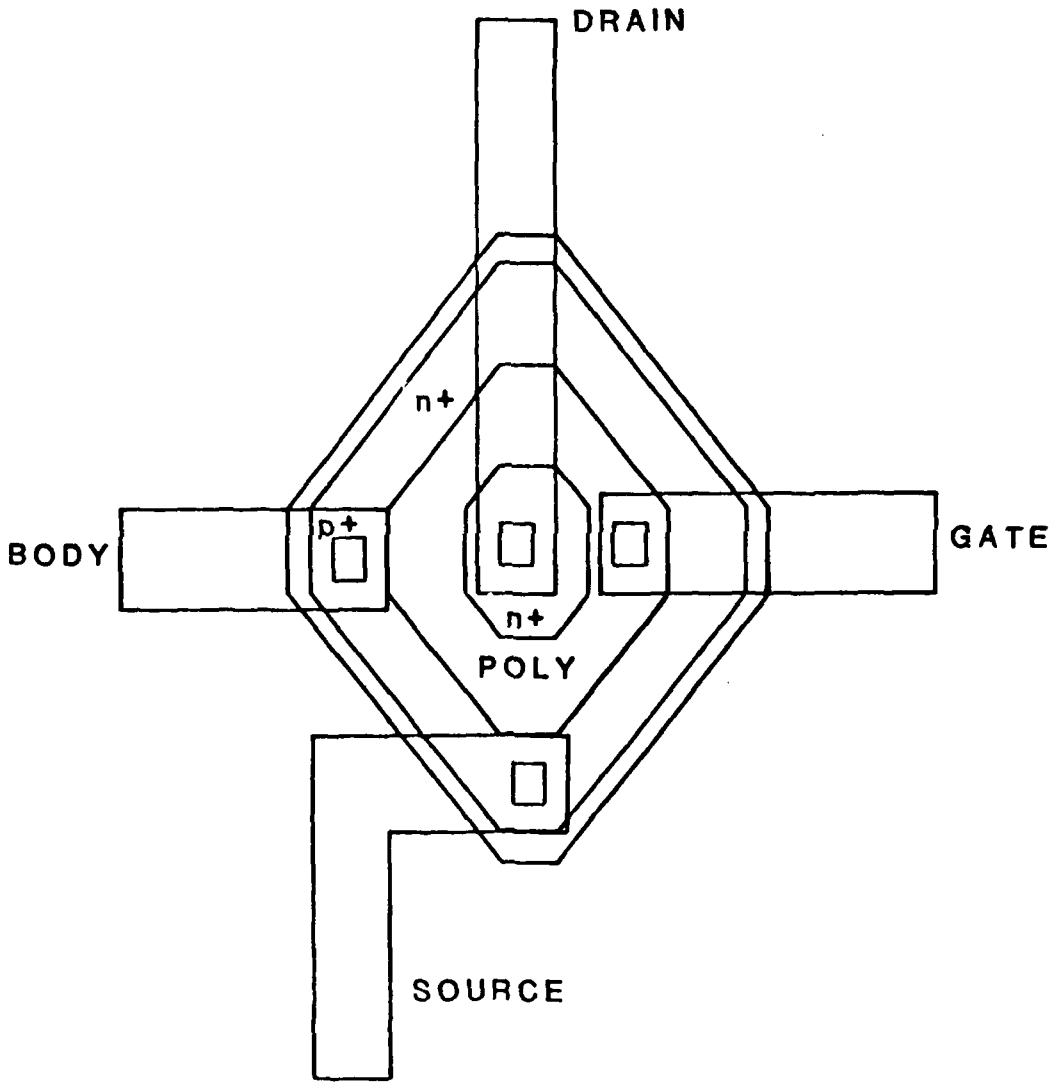


Figure 4. SOI MOSFET, Round Gate Structure

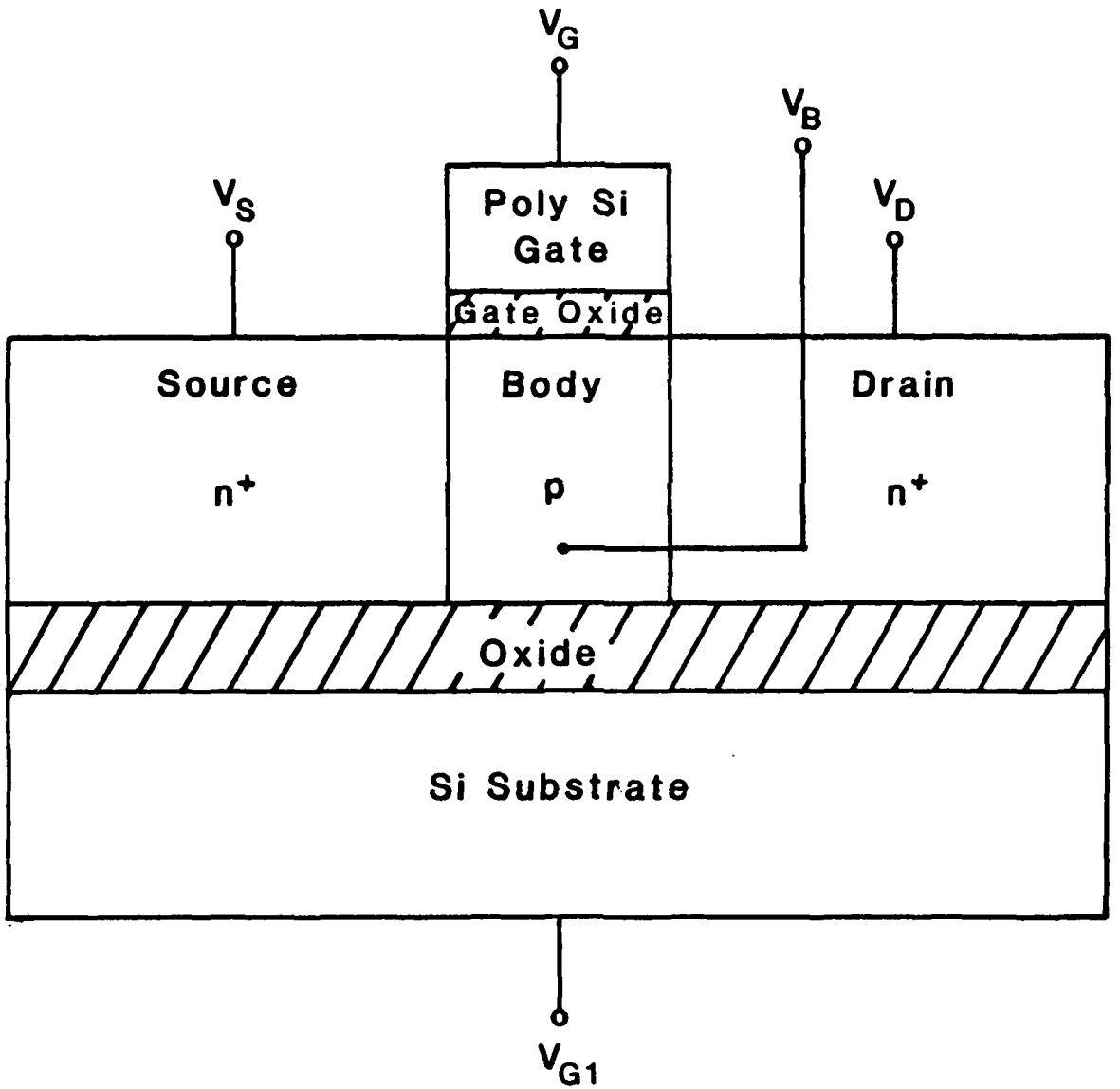


Figure 5. Typical Cross Sectional View of a SOI MOSFET with Terminal Connections

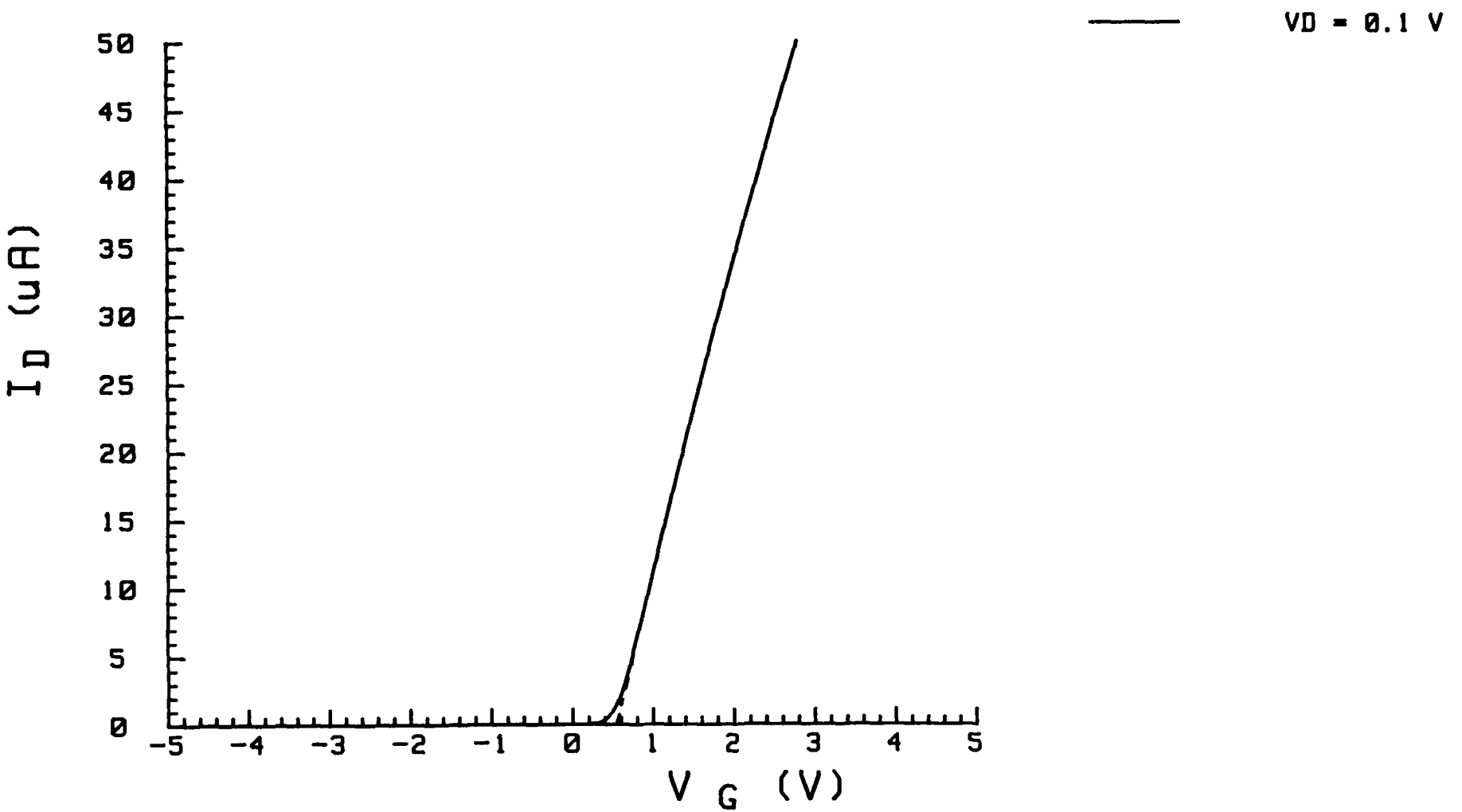


Figure 6. Threshold Voltage Calculation of a Type A Device Operating in the Linear Region. V_{G1}=-5V, V_{DS}=0.1V

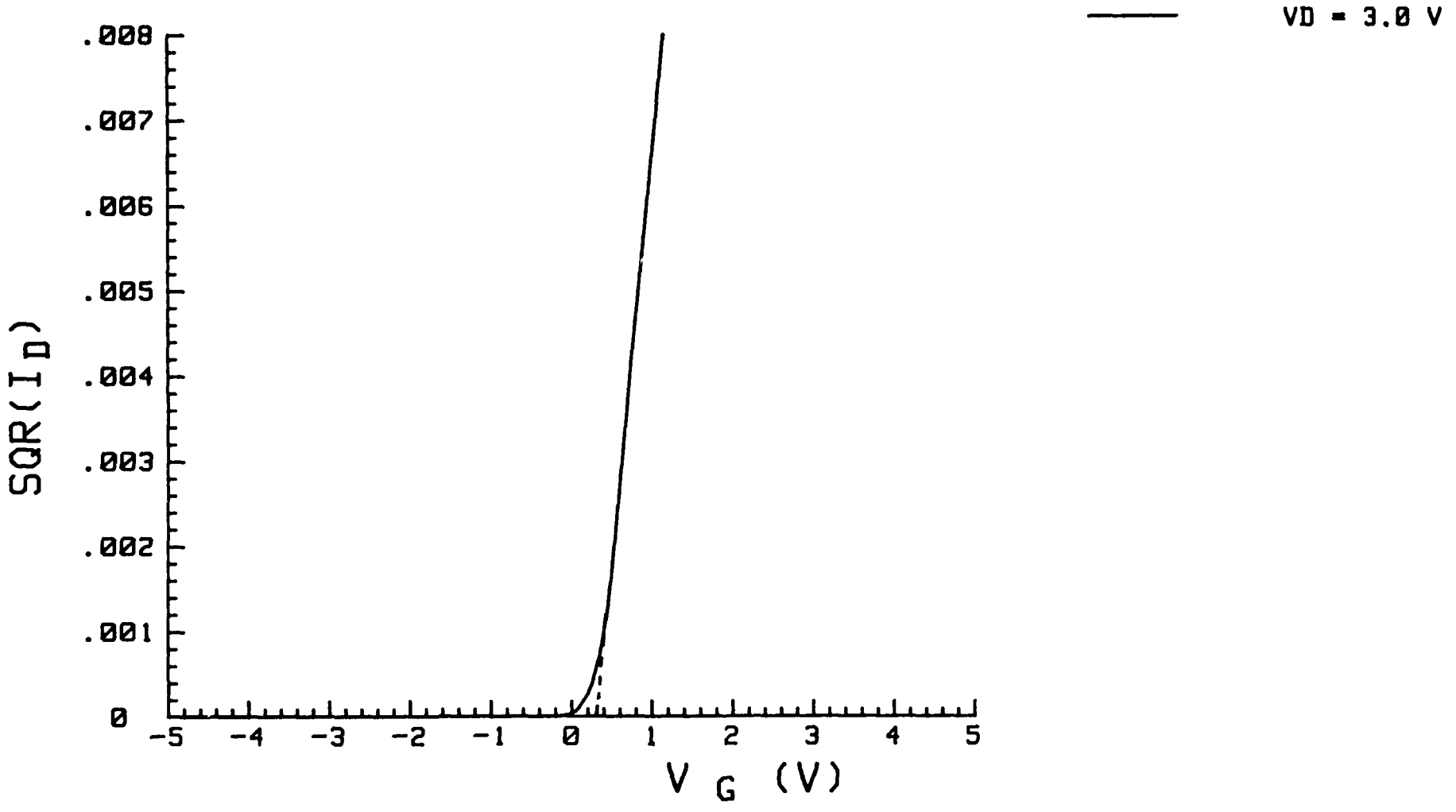


Figure 7. Threshold Voltage Calculation of a Type A Device Operating in the Saturation Region. V_{G1}=-5V, V_{DS}=3.0V

CHANGE IN THRESHOLD VOLTAGE AS A FUNCTION OF TOTAL DOSE

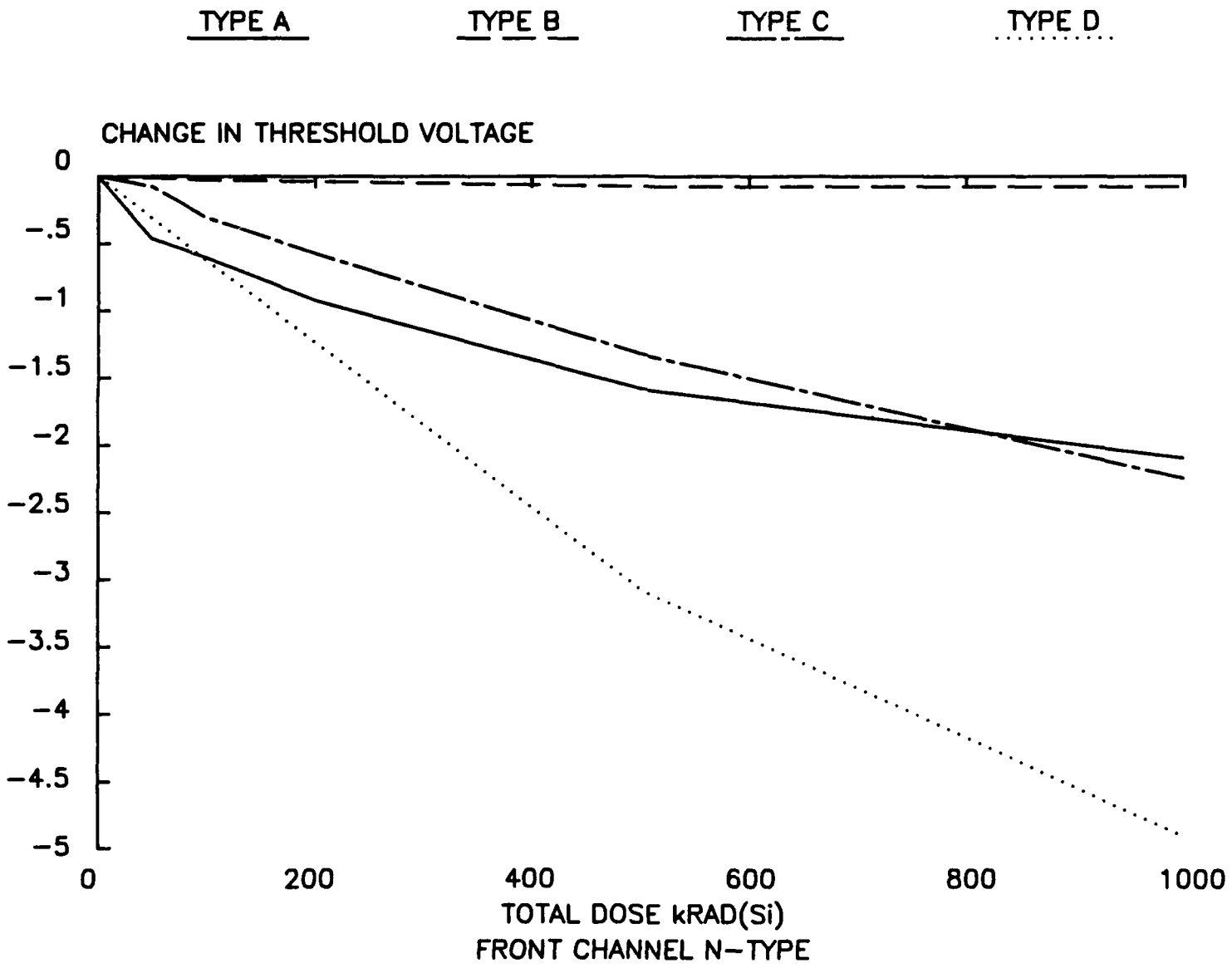


Figure 8.A

CHANGE IN THRESHOLD VOLTAGE AS A FUNCTION OF TOTAL DOSE

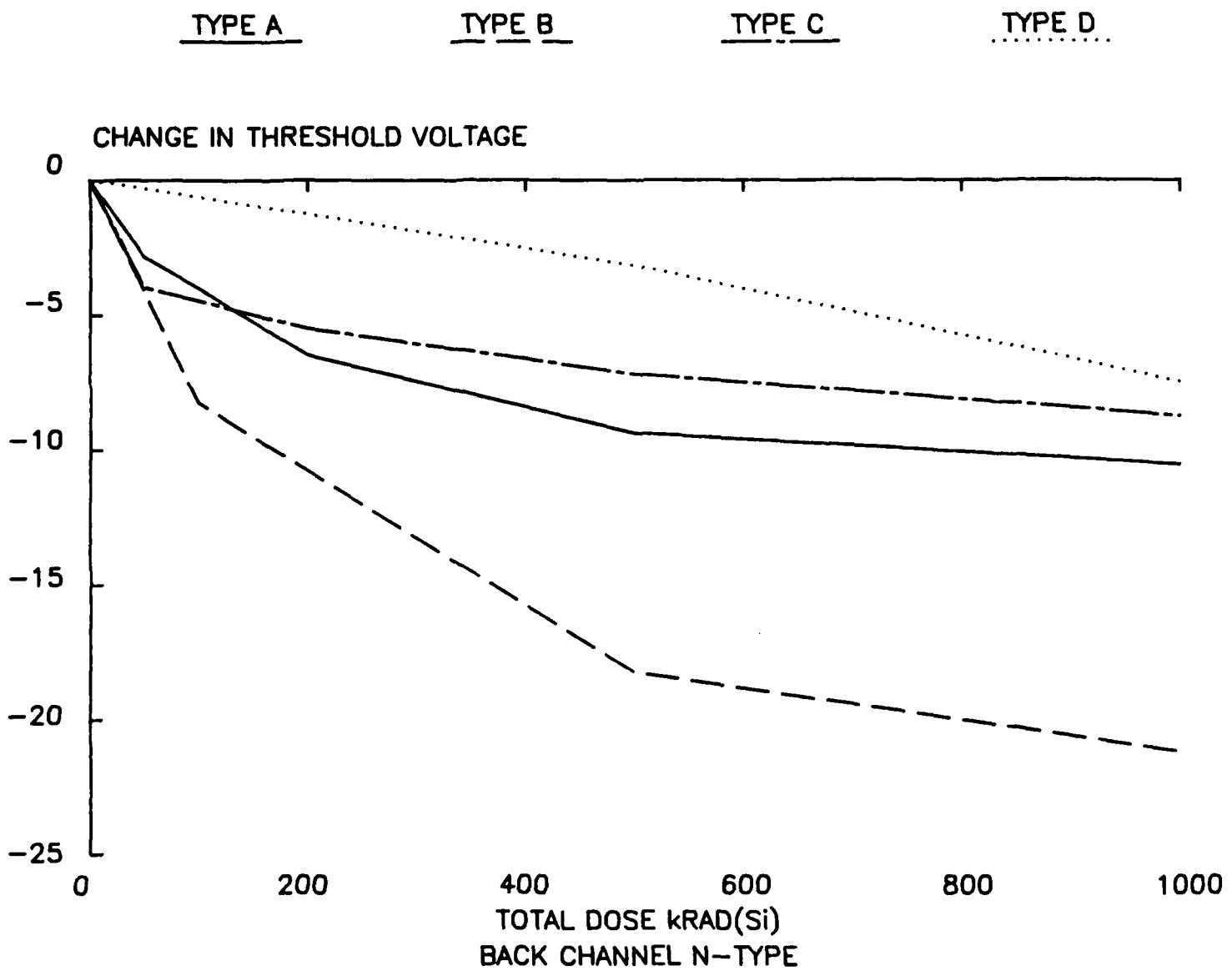


Figure 8.B

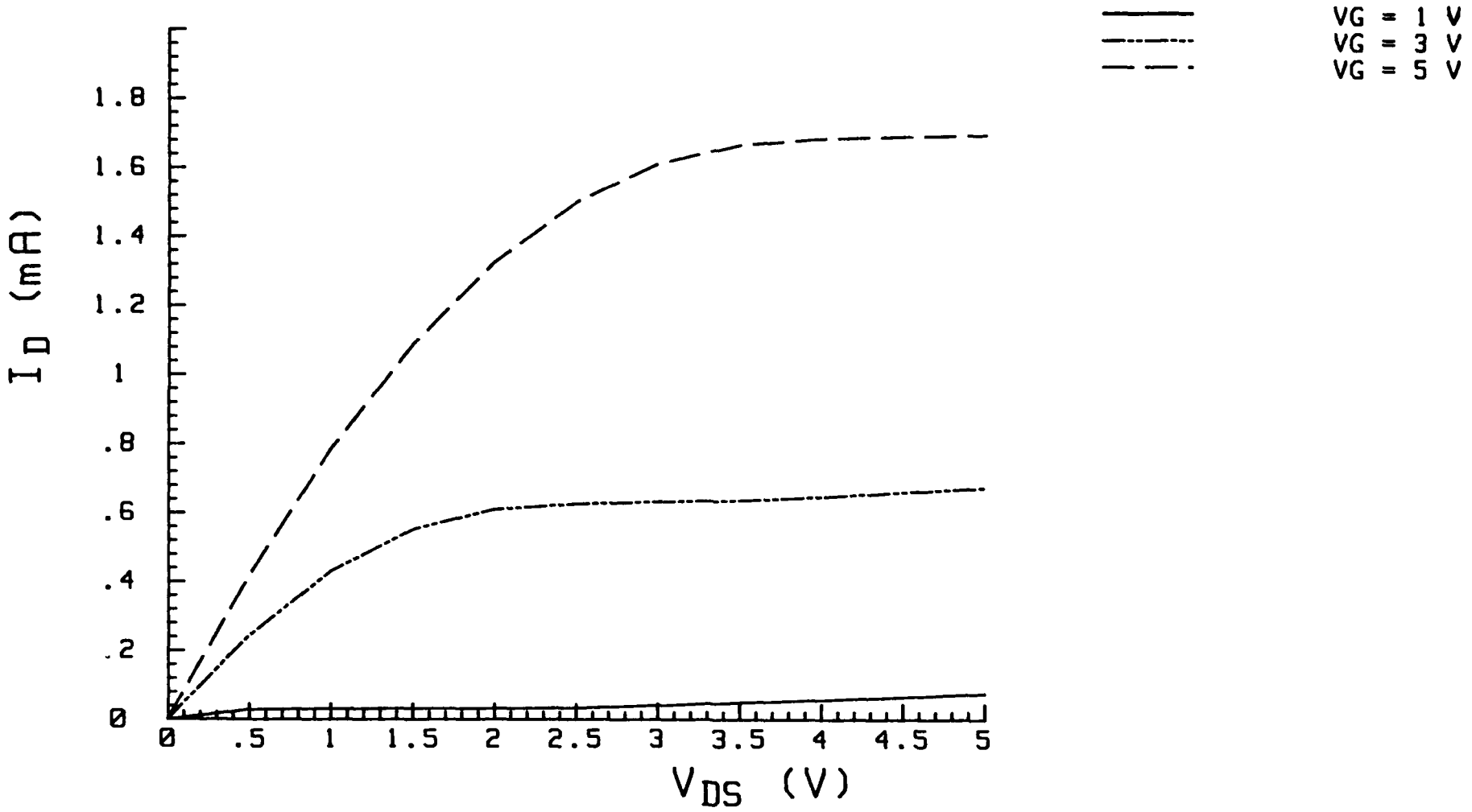


Figure 9.A Pre-radiation Front Gate I_D-V_D Characteristics of a 5um n-channel SOI MOSFET (Type A).
V_{G1} (Back Gate) = -5V
V_{G1}=-5V during irradiation

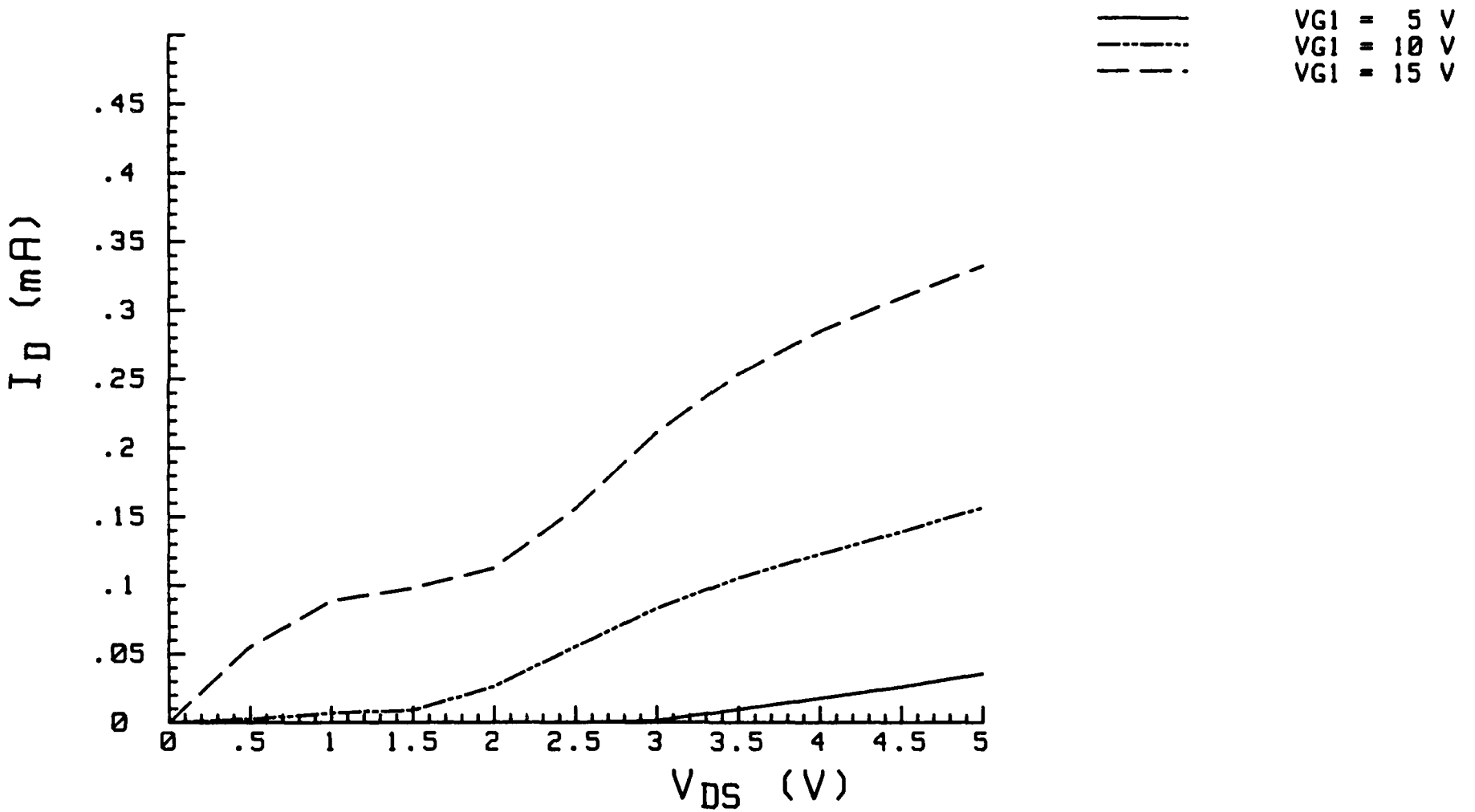


Figure 9.B Pre-radiation Back Gate I_D-V_D Characteristics of a 5um n-channel SOI MOSFET (Type A).
V_G=-5V
V_{G1}=-5V during irradiation

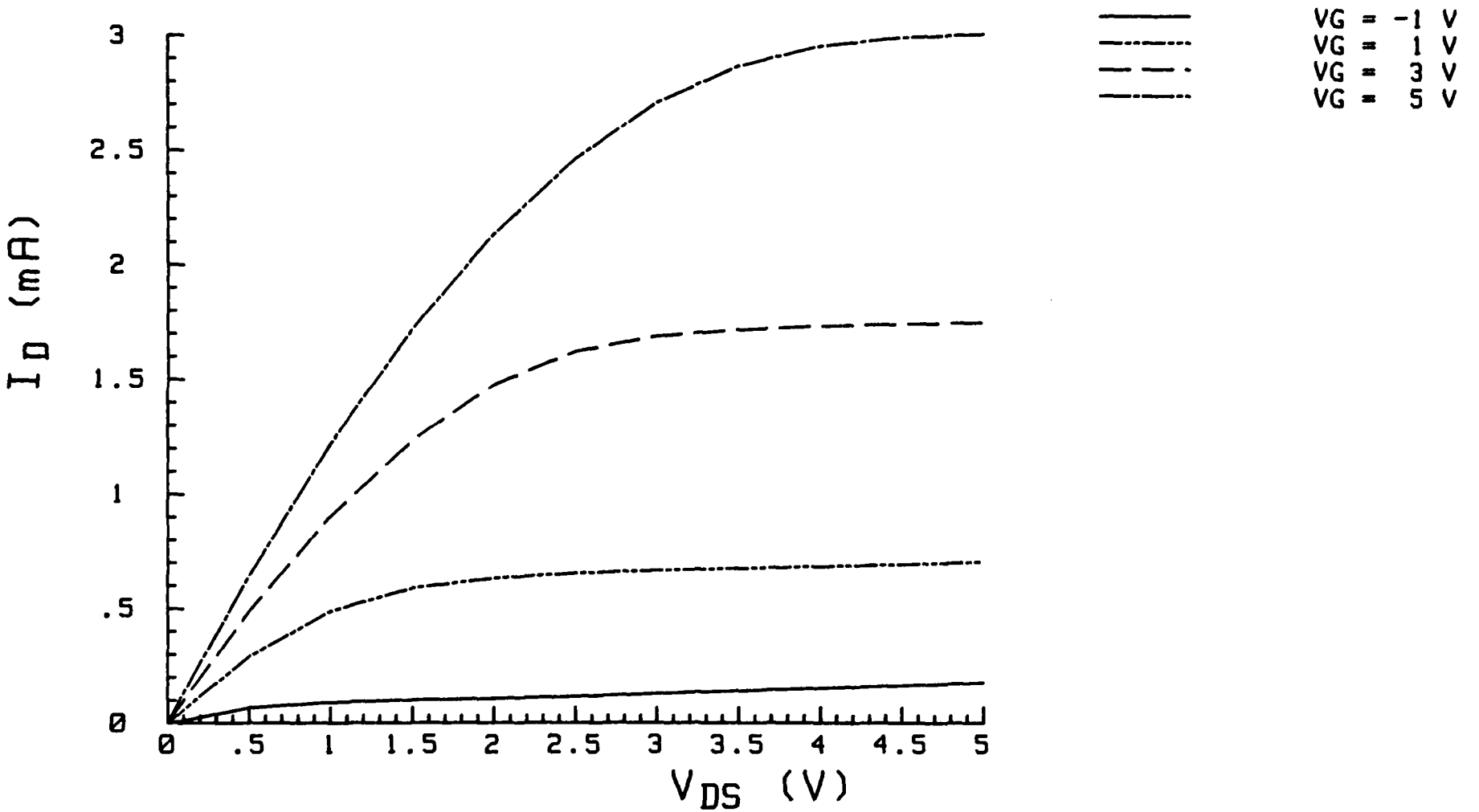


Figure 10.A Total Dose Response of Front Gate I_D-V_D Characteristics of a 5um n-channel SOI MOSFET (Type A).
V_{G1} (Back Gate) = -5V
V_{G1}=-5V during irradiation

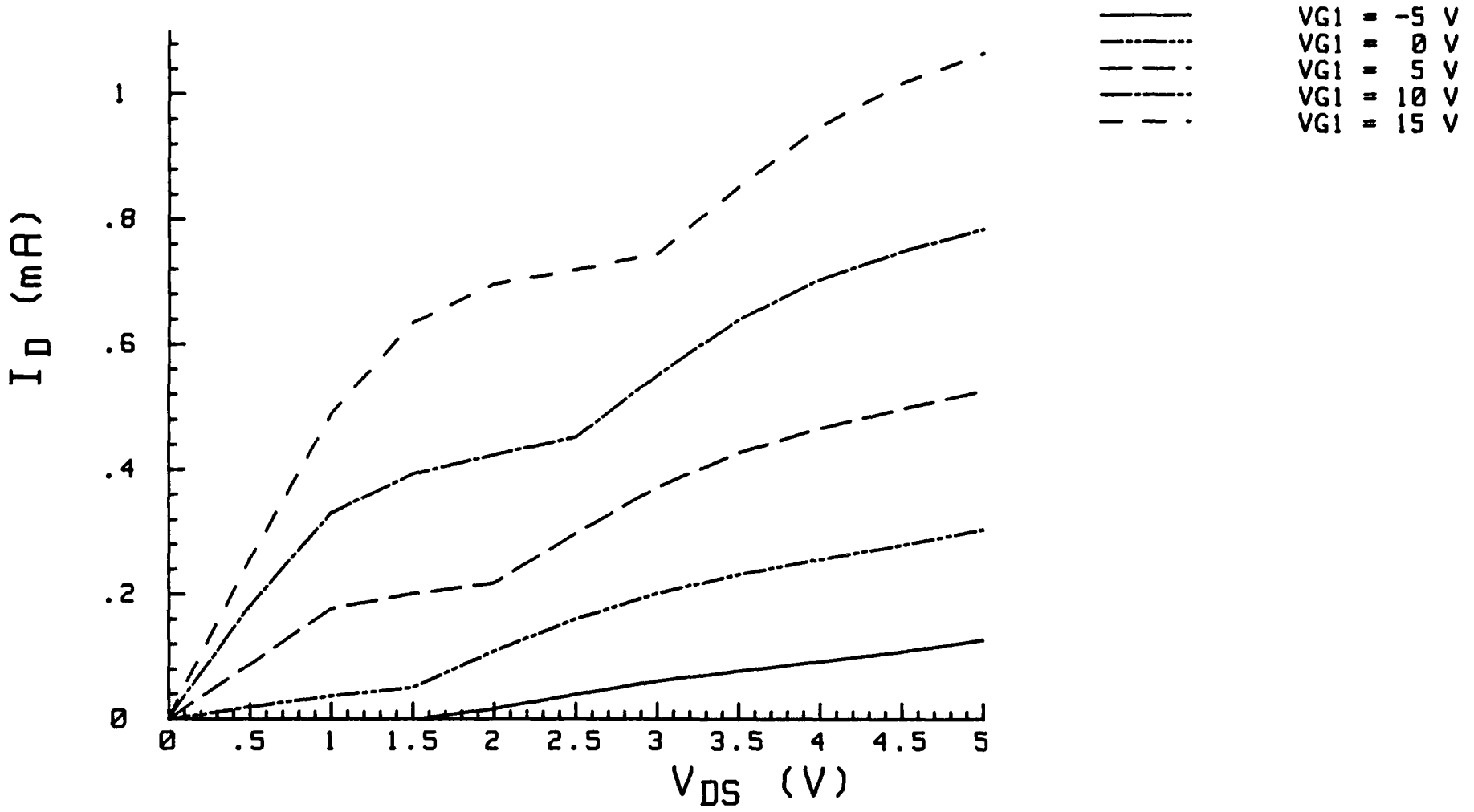


Figure 10.B Total Dose Response of Back Gate I_D-V_D Characteristics of a 5um n-channel SOI MOSFET (Type A).
V_G=-5V
V_{G1}=-5V during irradiation

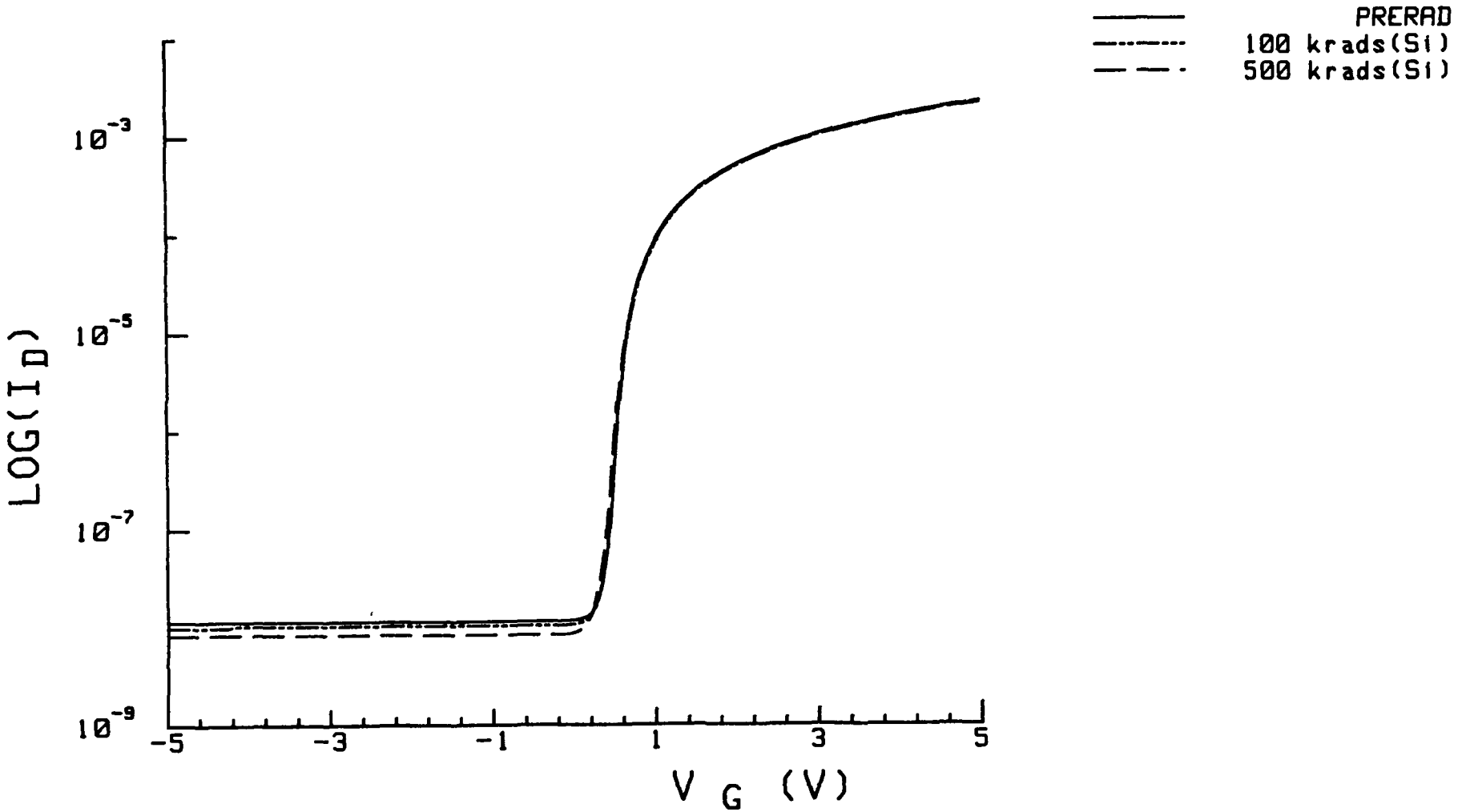


Figure 11.A Total Dose Response of Front Gate Subthreshold I_D-V_G Characteristics of an H-gate 1.2um n-channel SOI MOSFET (Type B).
V_D=5V, V_{G1} (Back Gate) = -20V
V_{G1}=0V during irradiation

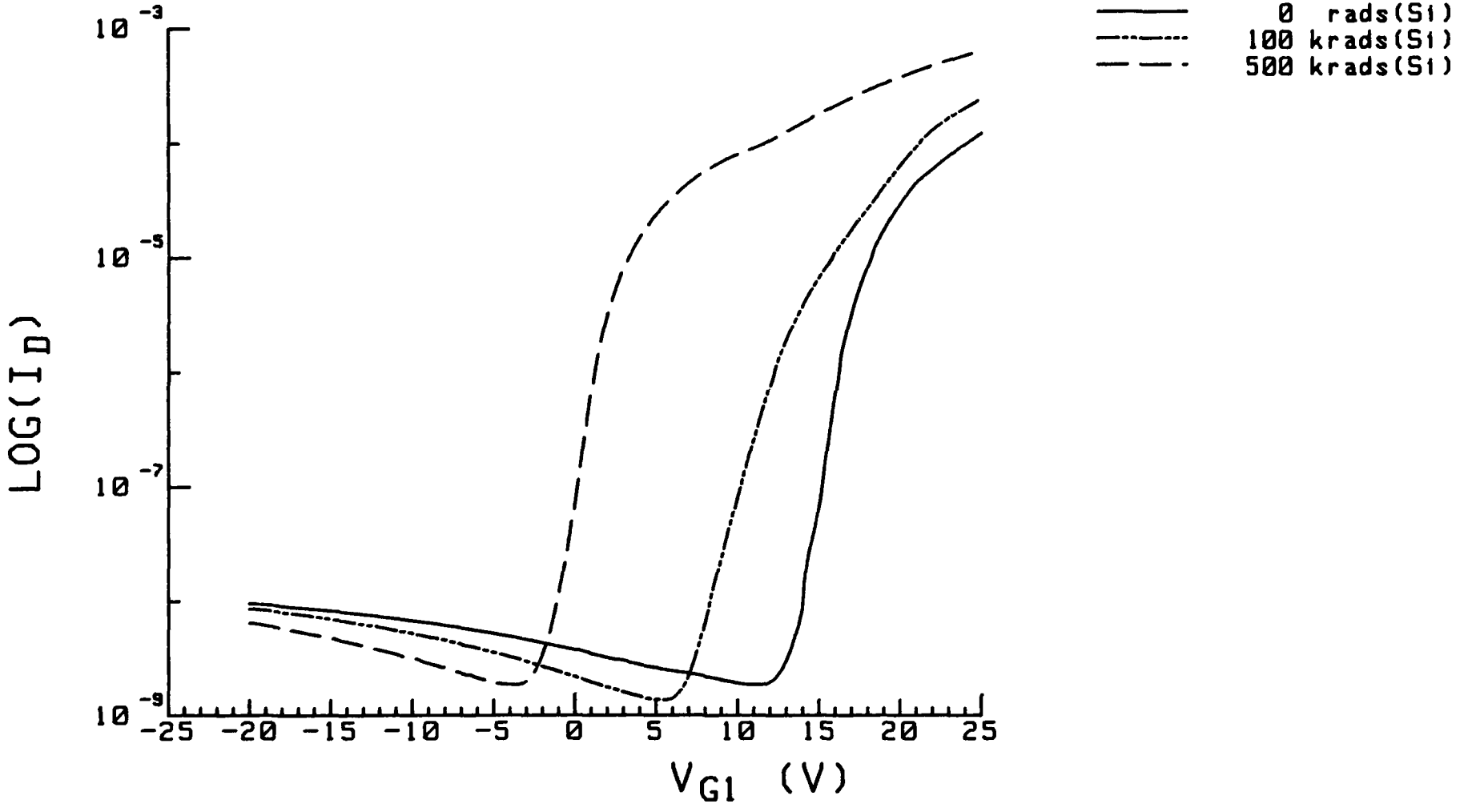


Figure 11.B Total Dose Response of Back Gate Subthreshold I_D-V_{G1} Characteristics of an H-gate 1.2um n-channel SOI MOSFET (Type B).
V_D=5V, V_G=-5V
V_{G1}= 0V during irradiation

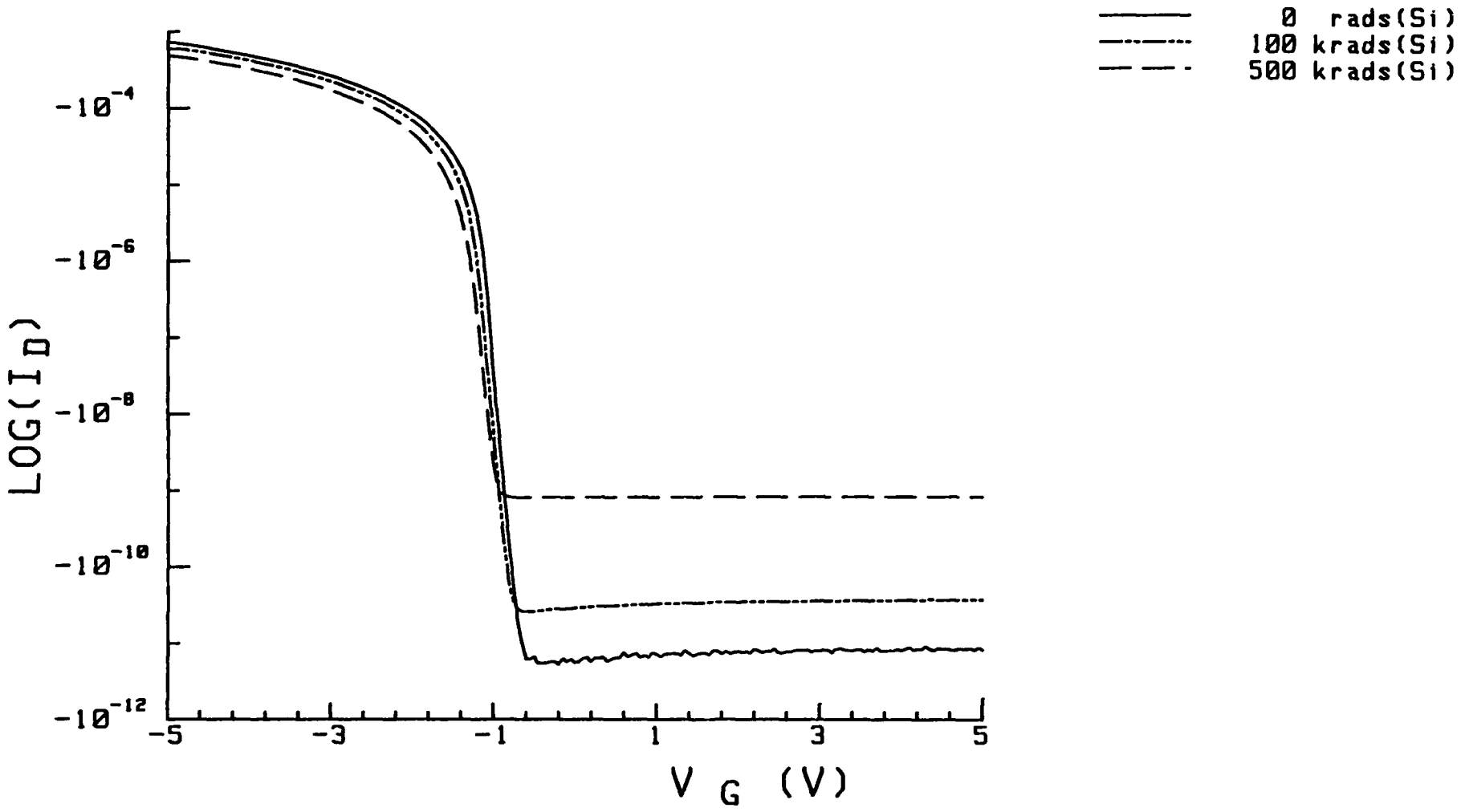


Figure 12.A Total Dose Response of Front Gate Subthreshold I_D-V_G Characteristics of an H-gate 1.2um p-channel SOI MOSFET (Type B).
V_D=-5V, V_{G1} (Back Gate) = 3V
V_{G1}= 0V during irradiation

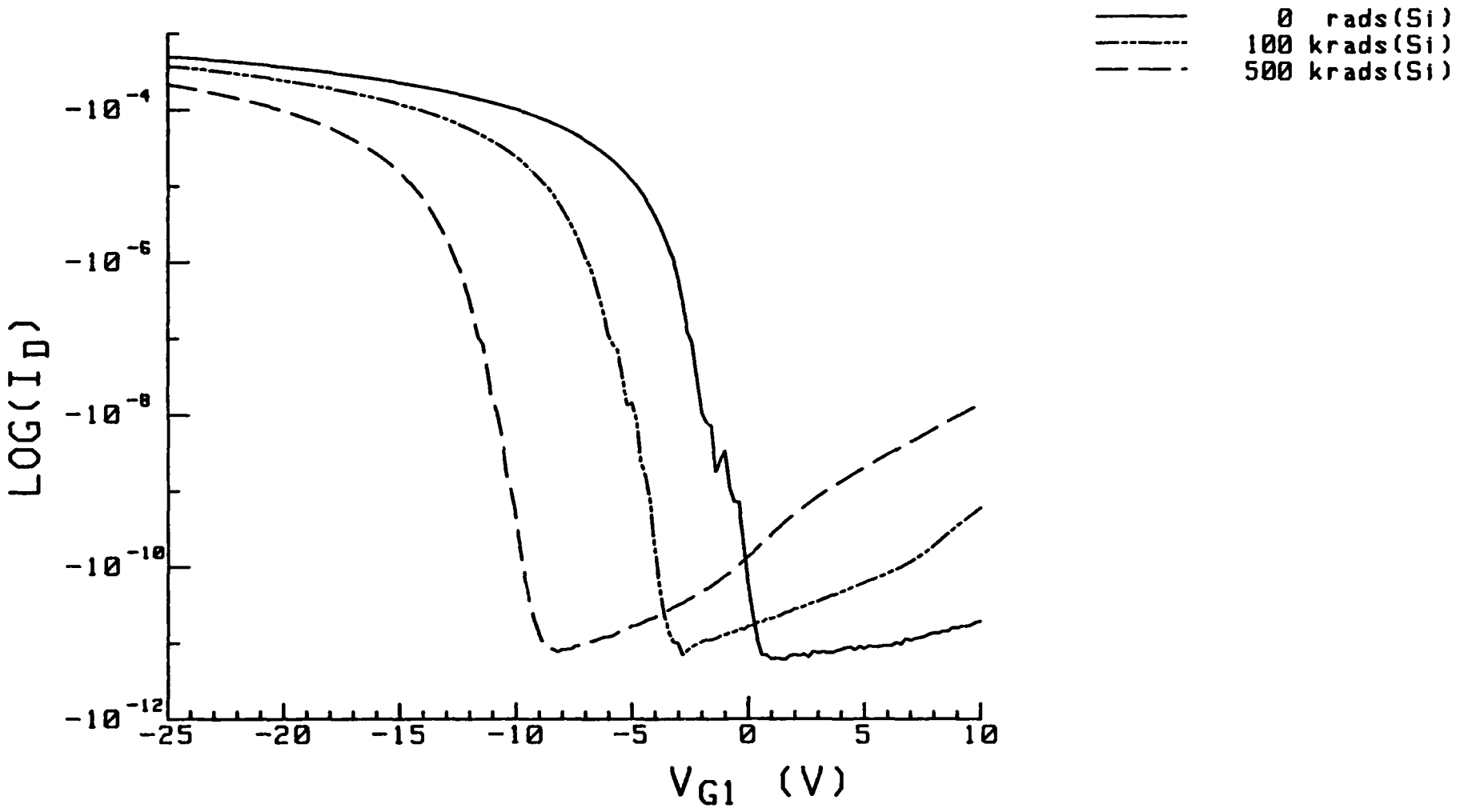


Figure 12.B Total Dose Response of Back Gate Subthreshold I_D-V_{G1} Characteristics of an H-gate 1.2um p-channel SOI MOSFET (Type B).
V_D=-5V, V_G=3V
V_{G1}= 0V during irradiation

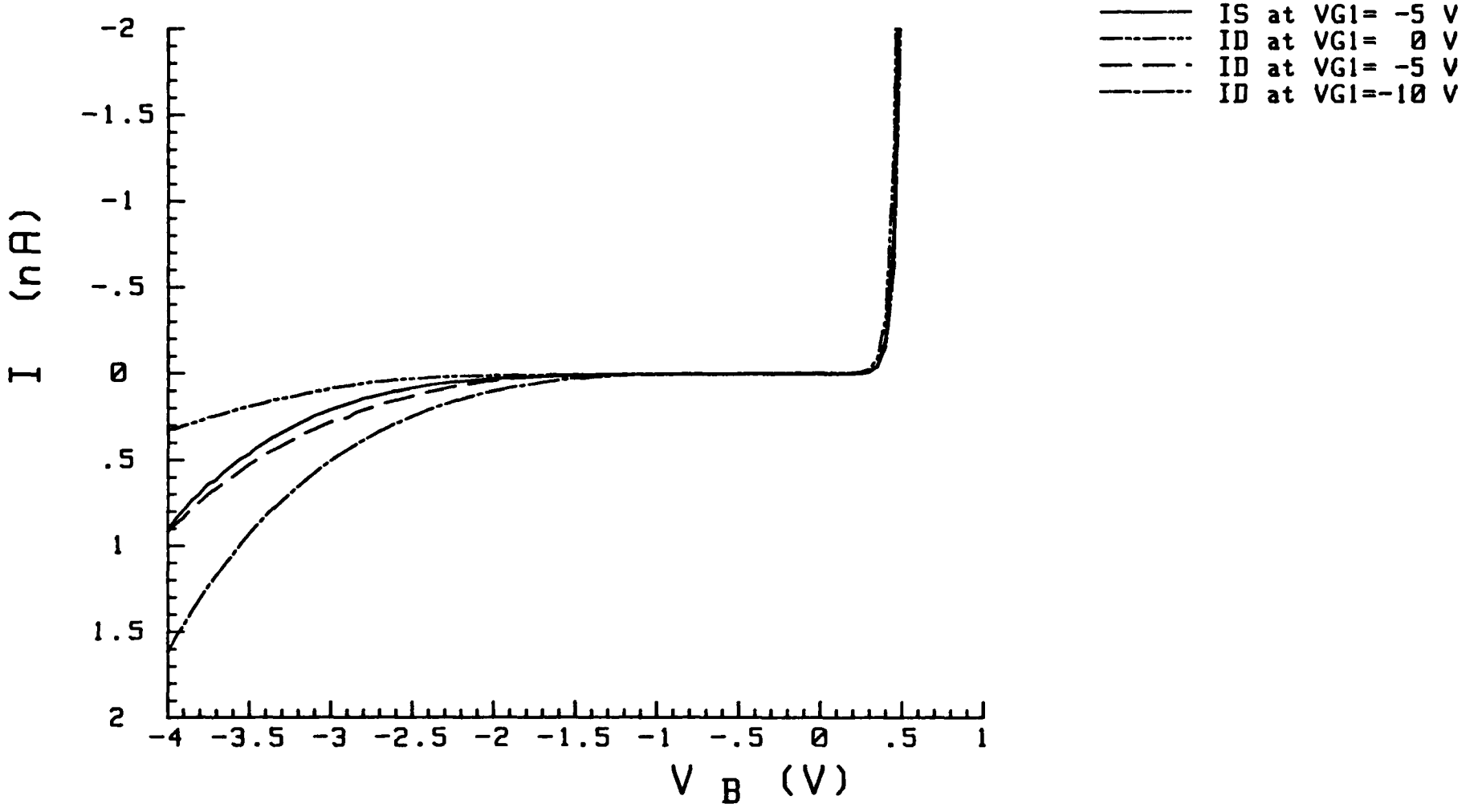


Figure 13. Body-Drain (p-n) and Body-Source (p-n) Junctions Diode Characteristics of an H-gate 1.2um n-channel SOI MOSFET with Body Contact (Type B).
$V_G=V_{G1}=-5V$

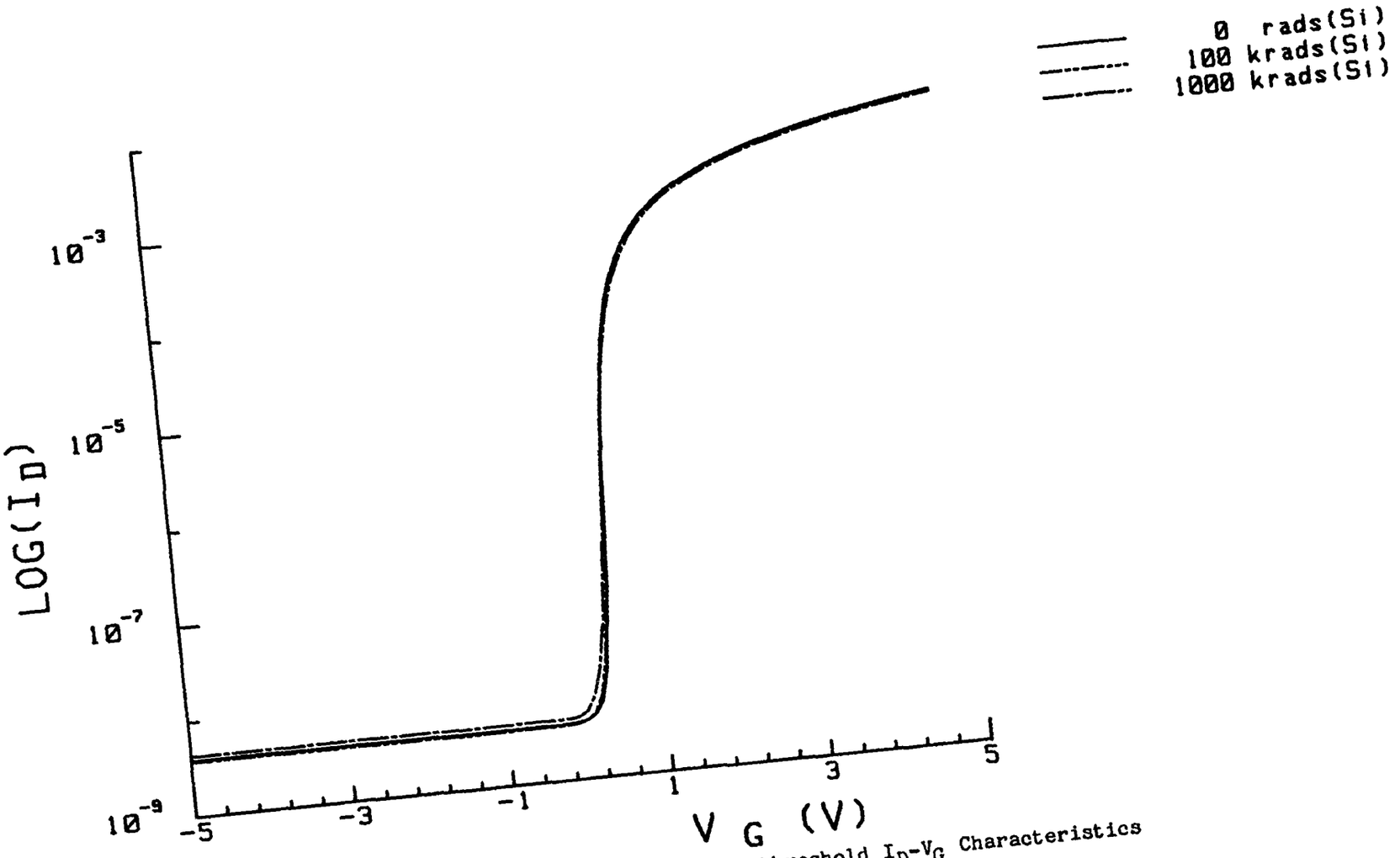


Figure 14.A Total Dose Response of Front Gate Subthreshold I_D-V_G Characteristics of an Enclosed Gate 1.2um n-channel SOI MOSFET (Type B).
V_D=5V, V_{G1} (Back Gate) = -20V
V_{G1}= 0V during irradiation

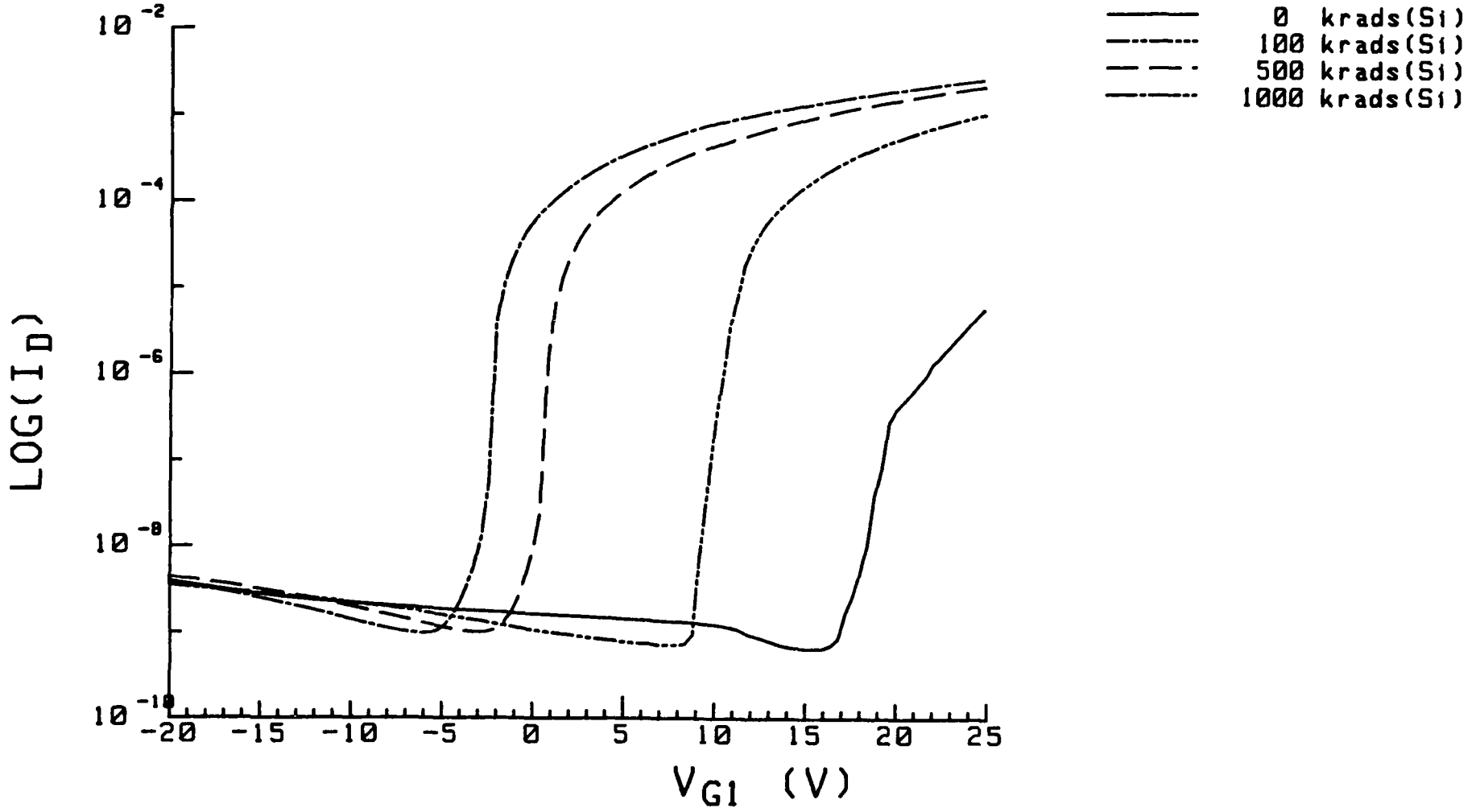


Figure 14.B Total Dose Response of Back Gate Subthreshold I_D-V_{G1} Characteristics of an Enclosed Gate 1.2um n-channel SOI MOSFET (Type B).
V_D=5V, V_G=-5V
V_{G1}= 0V during irradiation

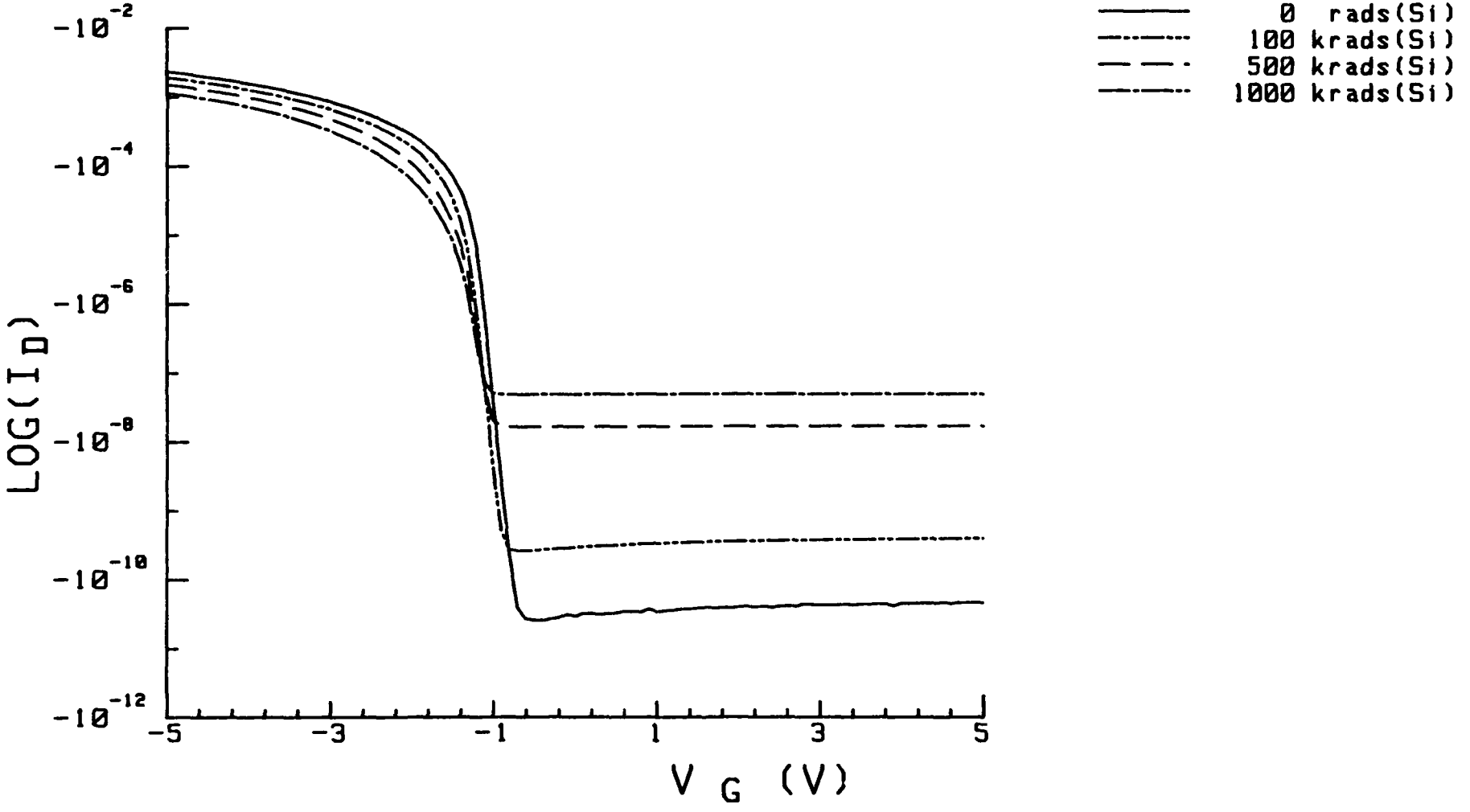


Figure 15.A Total Dose Response of Front Gate Subthreshold I_D-V_G Characteristics of an Enclosed Gate 1.2um p-channel SOI MOSFET (Type B).
V_D=-5V, V_{G1} (Back Gate) = 3V
V_{G1}= 0V during irradiation

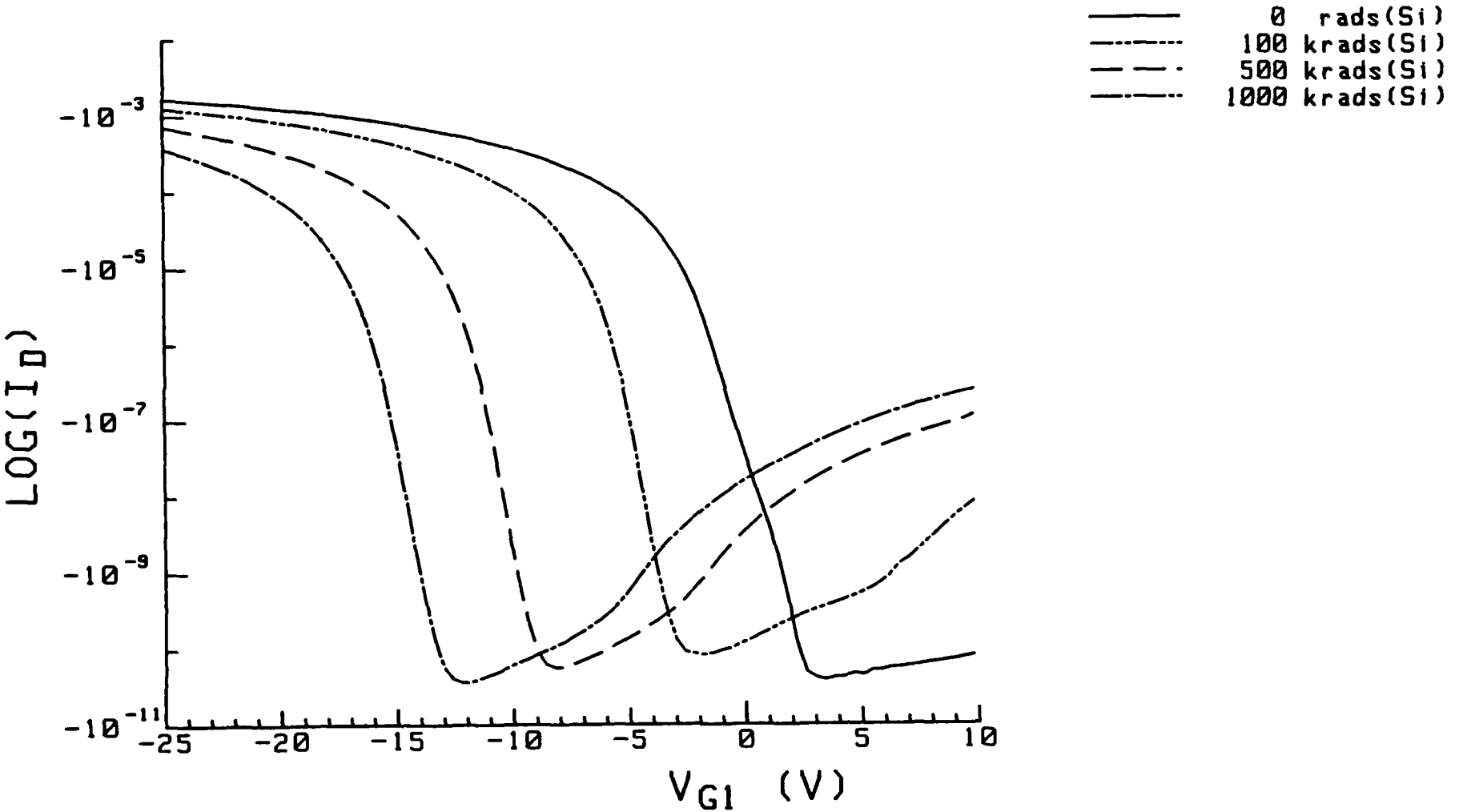


Figure 15.B Total Dose Response of Back Gate Subthreshold I_D-V_{G1} Characteristics of an Enclosed Gate 1.2um p-channel SOI MOSFET (Type B).
V_D=-5V, V_G=3V
V_{G1}= 0V during irradiation

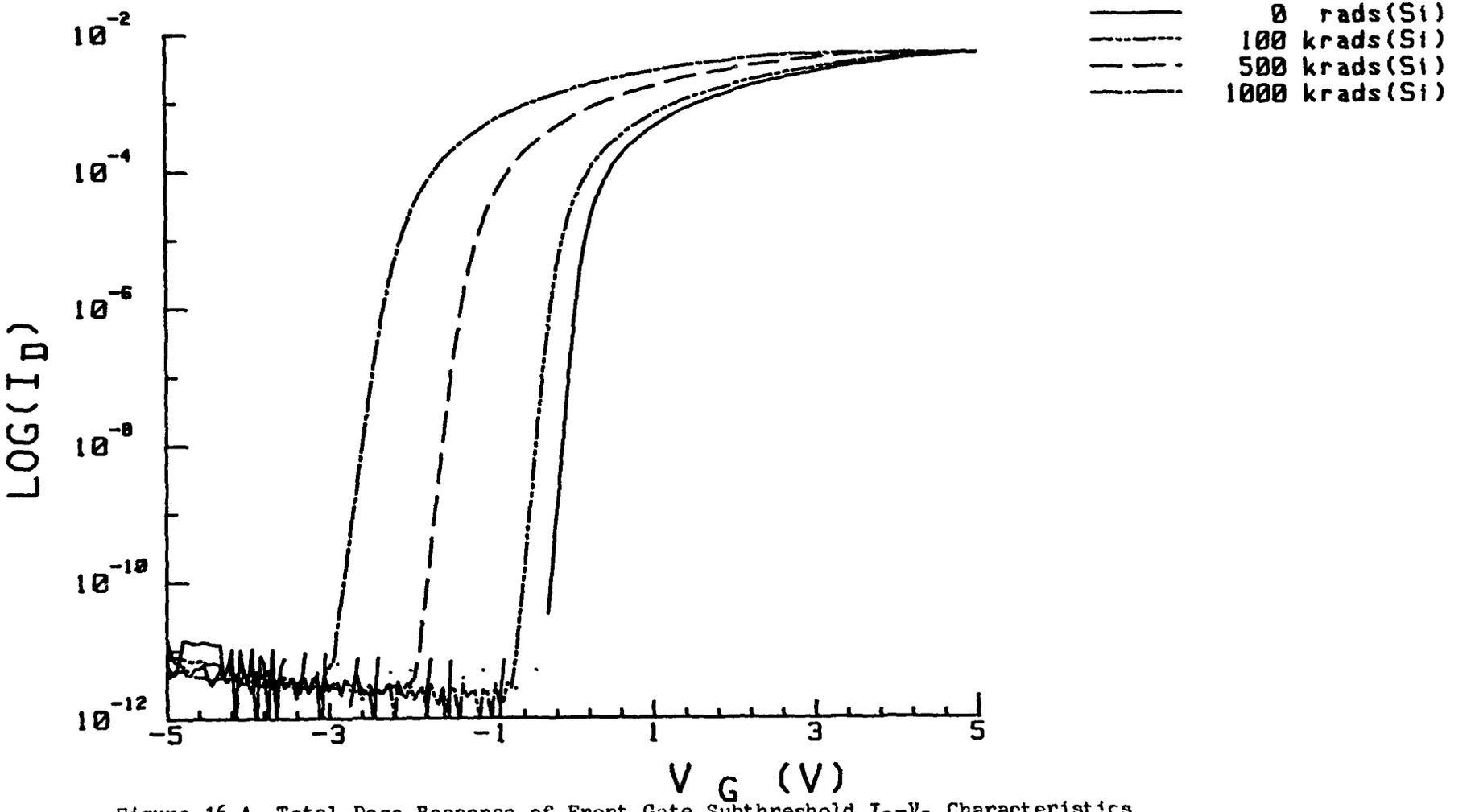


Figure 16.A Total Dose Response of Front Gate Subthreshold I_D-V_G Characteristics of a Round Gate 5um n-channel SOI MOSFET (Type C).
V_D=3V, V_{G1} (Back Gate) = -5V
V_{G1}= -5V during irradiation

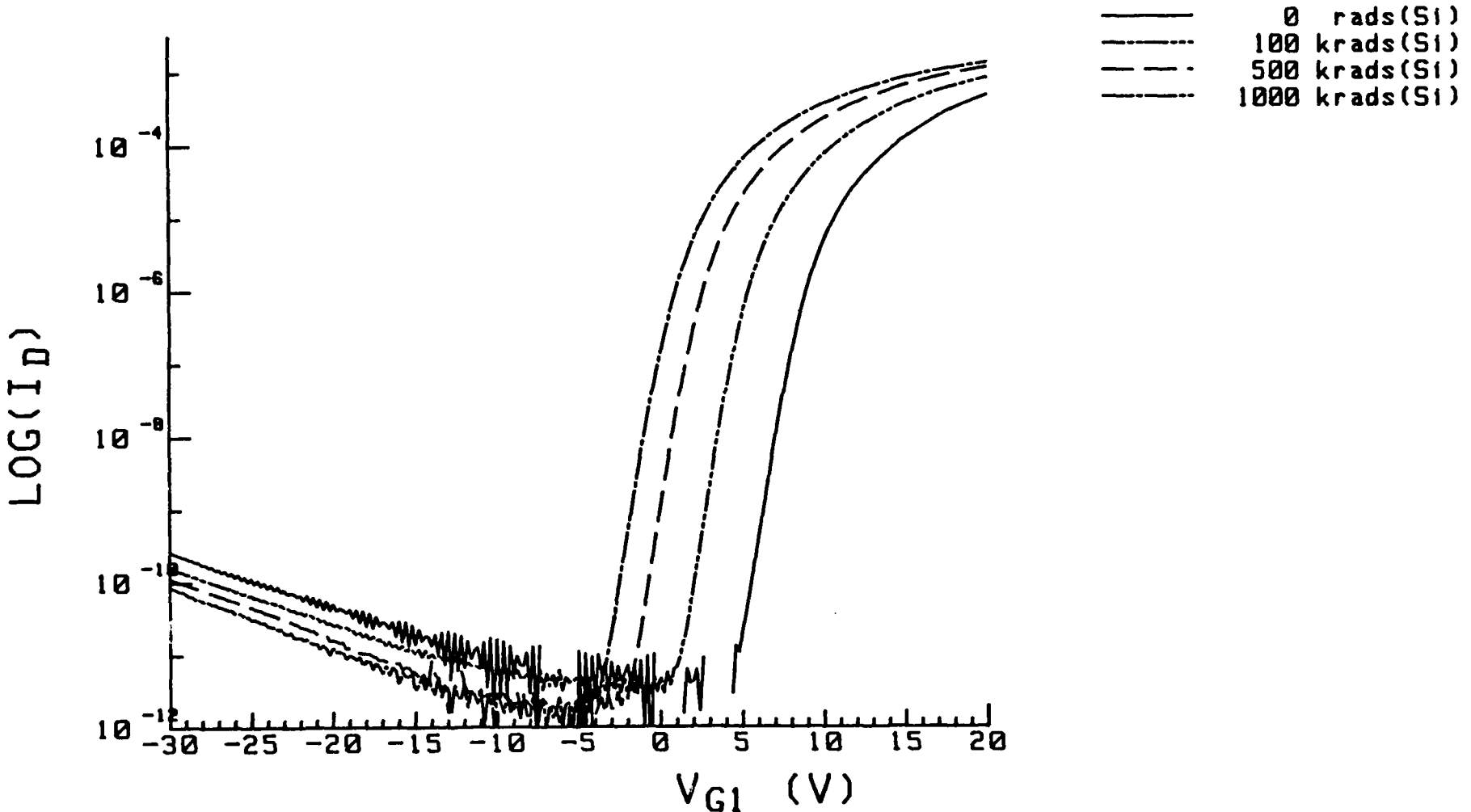


Figure 16.B Total Dose Response of Back Gate Subthreshold I_D-V_{G1} Characteristics of a Round Gate 5um n-channel SOI MOSFET (Type C).
V_D=3V, V_G=-5V
V_{G1}= -5V during irradiation

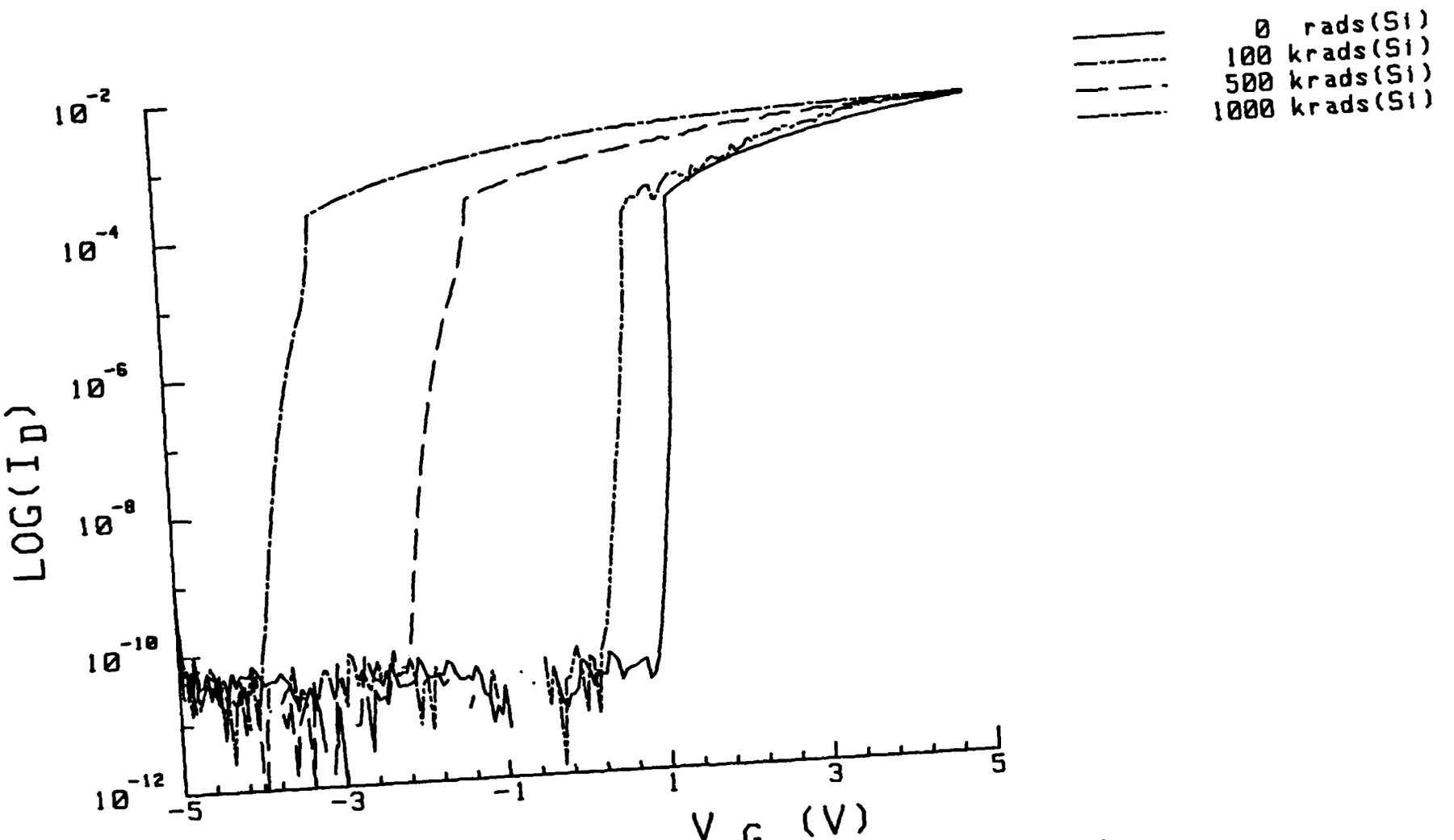


Figure 17.A Total Dose Response of Front Gate Subthreshold I_D-V_G Characteristics of an H-gate 3um n-channel ZMR SOI MOSFET (Type D).
V_D=3V, V_{G1} (Back Gate) = -20V
V_{G1}= -5V during irradiation

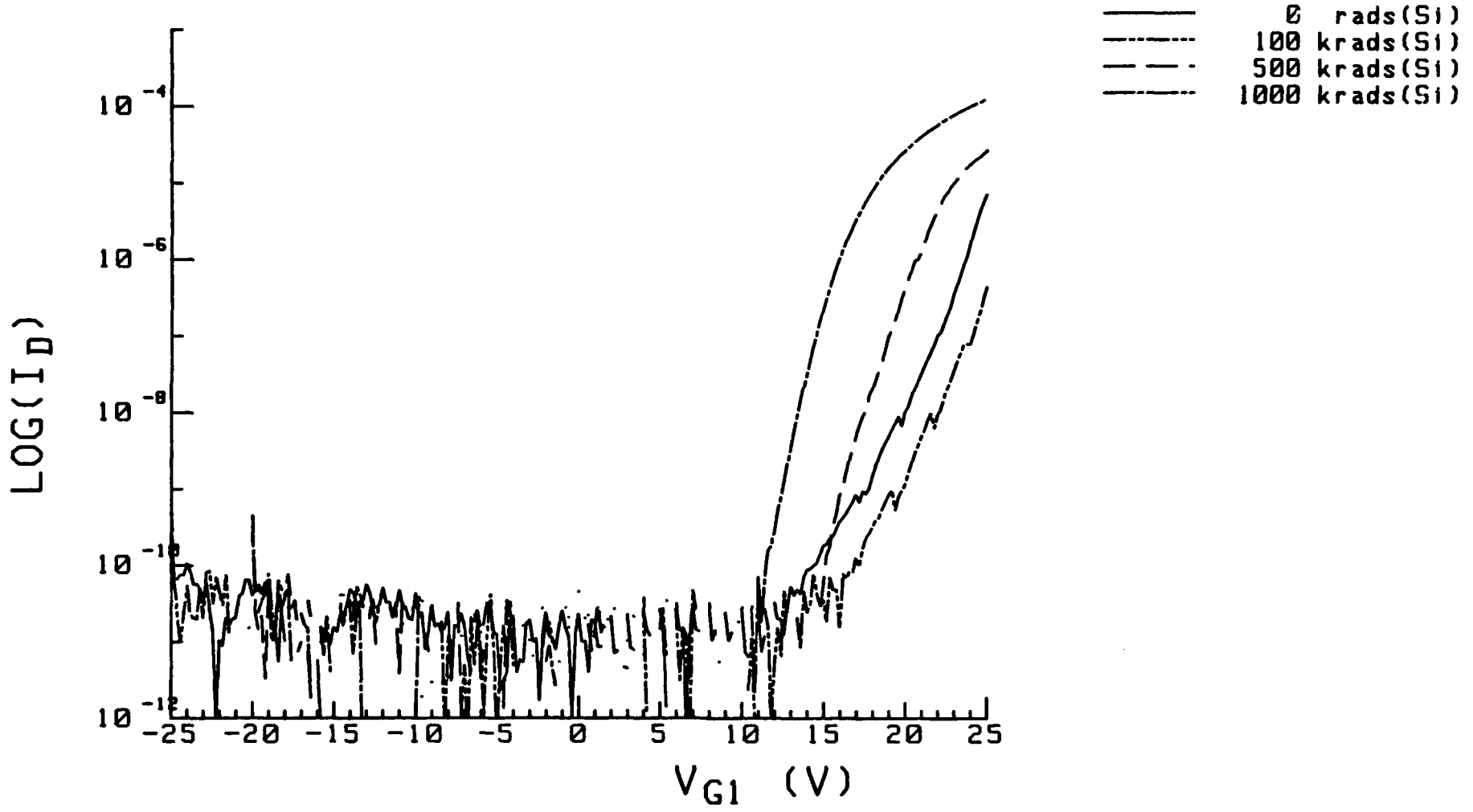


Figure 17.B Total Dose Response of Back Gate Subthreshold I_D-V_{G1} Characteristics of an H-gate 3um n-channel ZMR SOI MOSFET (Type D).
V_D=3V, V_G=-5V
V_{G1}=-5V during irradiation

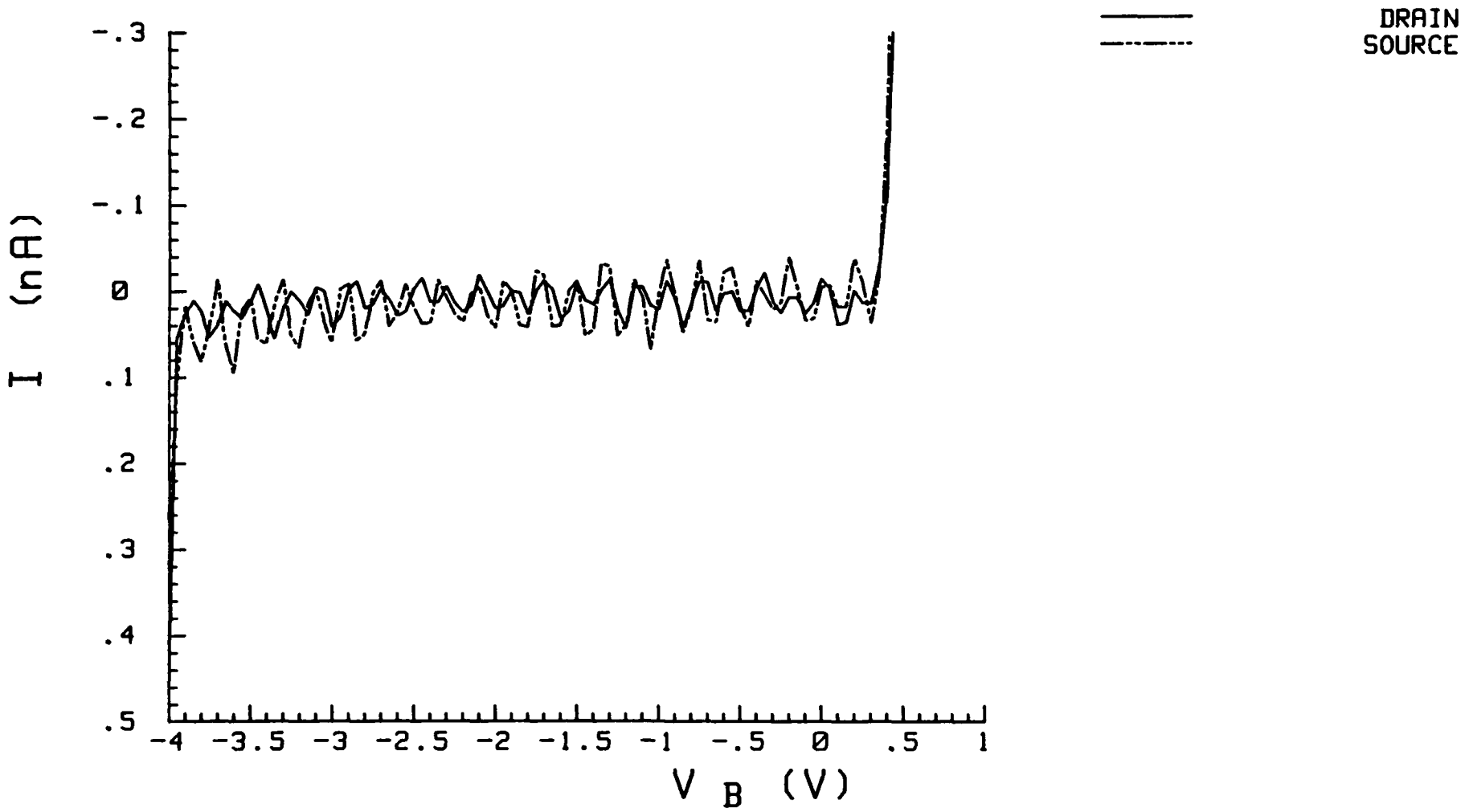


Figure 18. Body-Drain (p-n) and Body-Source (p-n) Junctions Diode Characteristics of an H-gate 3um n-channel ZMR SOI MOSFET with Body Contact (Type D). V_G=-5, V_{G1}=-20V

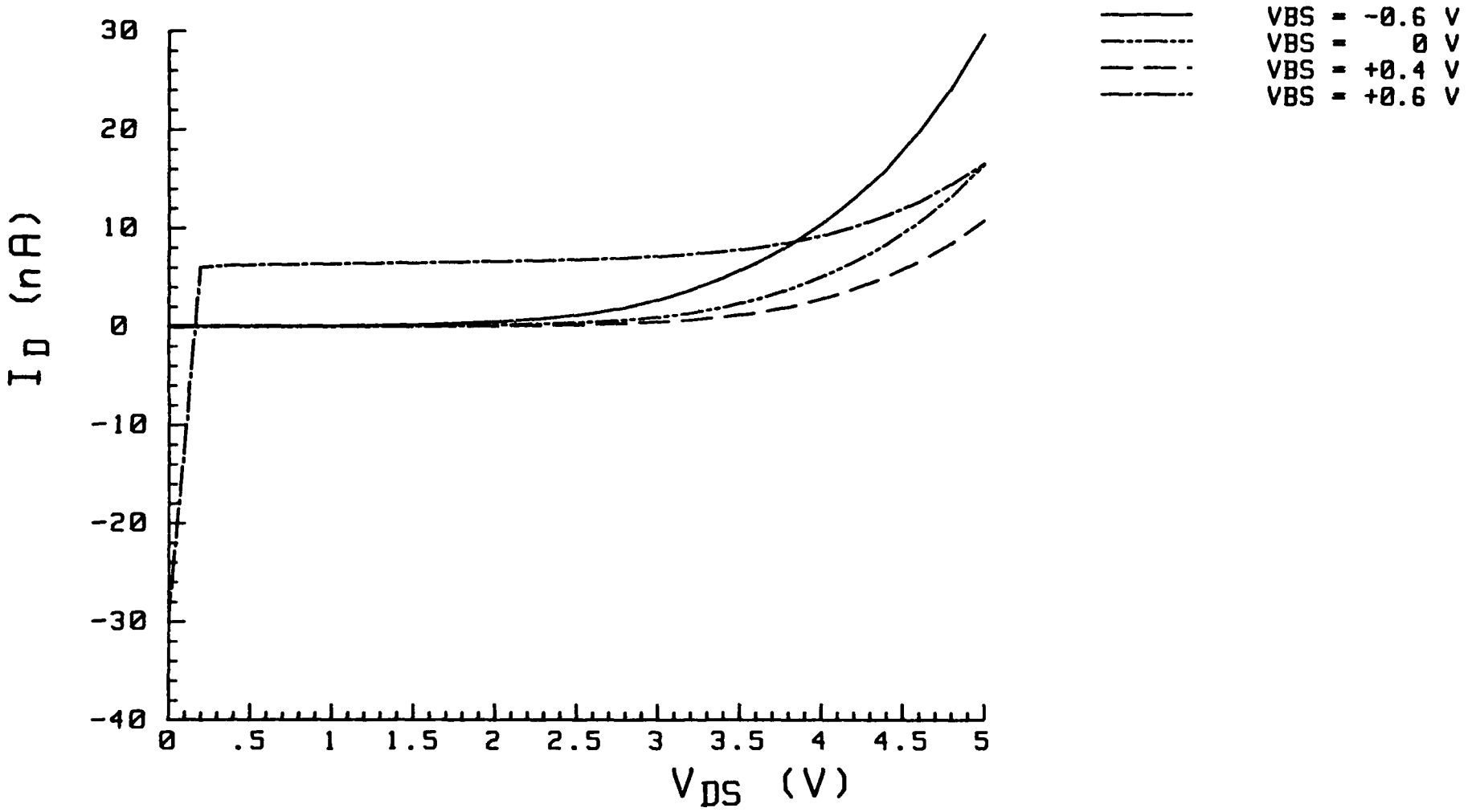


Figure 19.A I_D-V_{DS} Characteristics as a Function of V_{DS} of an H-gate 1.2um n-channel SOI MOSFET with Body Contact (Type B).
V_G=-3V, V_{G1}=-15V

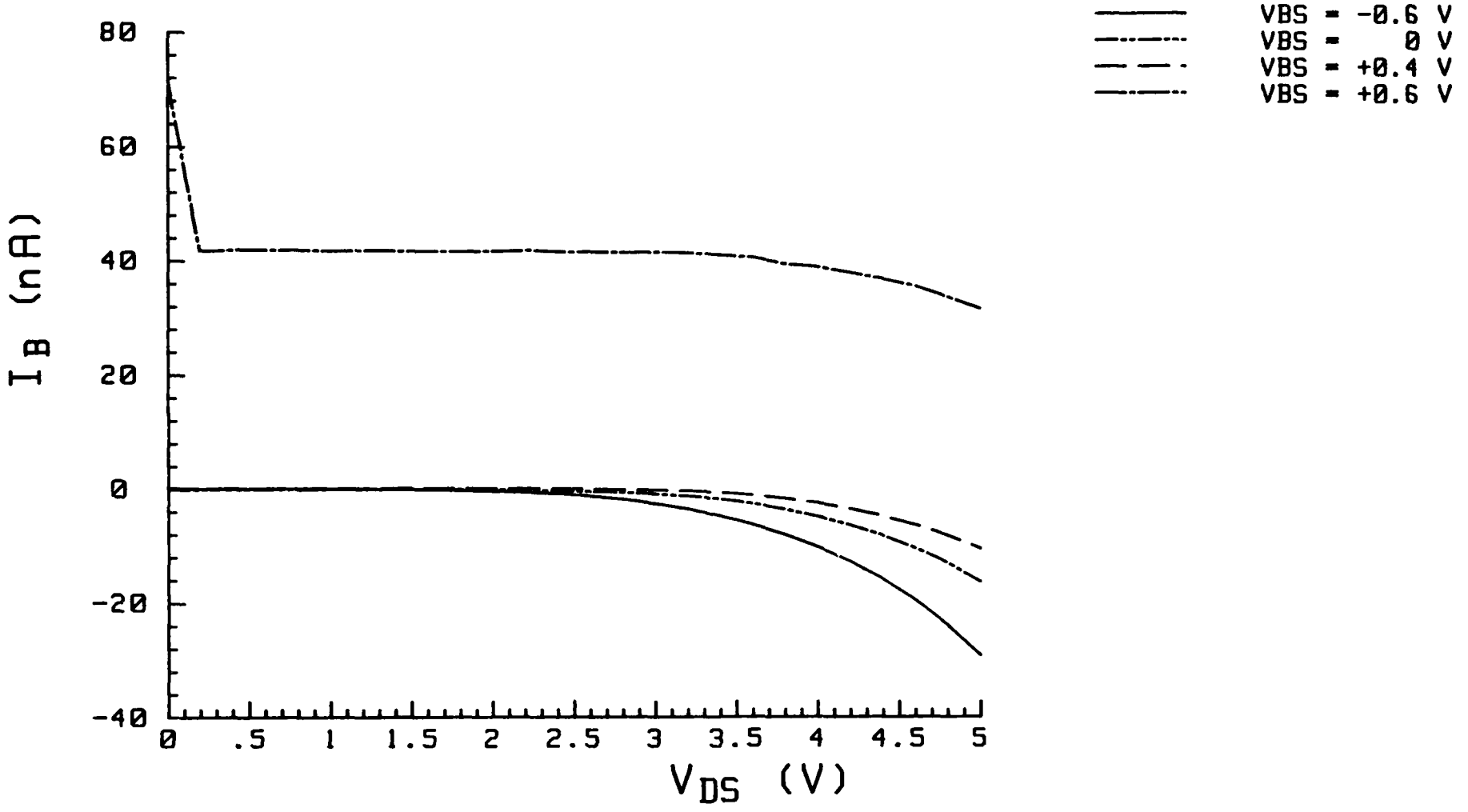


Figure 19.B I_B-V_{DS} Characteristics as a Function of V_{BS} of an H-gate 1.2um n-channel SOI MOSFET with Body Contact (Type B).
V_G=-3V, V_{G1}=-15V

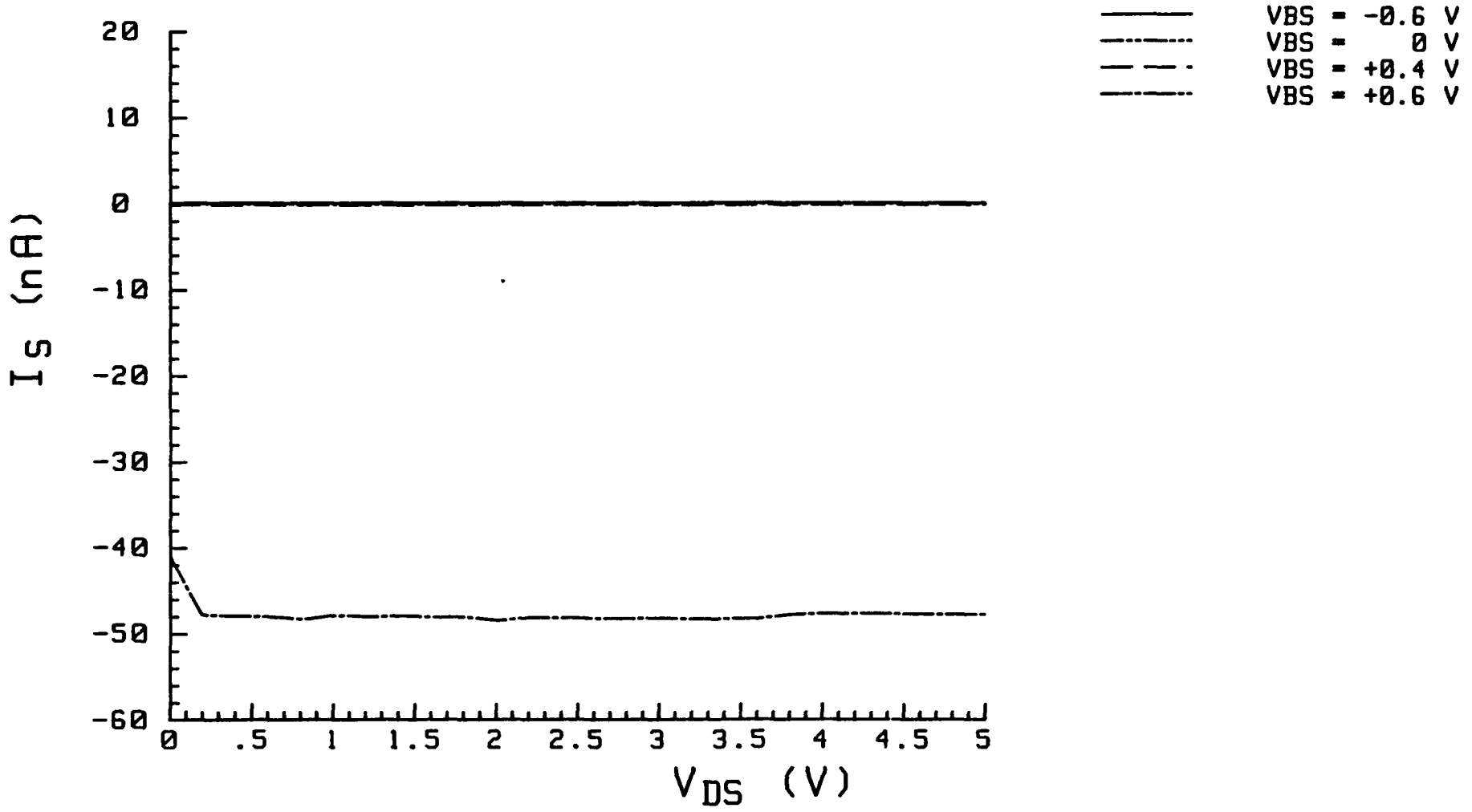


Figure 19.C I_S-V_{DS} Characteristics as a Function of V_{BS} of an H-gate 1.2um n-channel SOI MOSFET with Body Contact (Type B).
V_G=-3V, V_{G1}=-15V

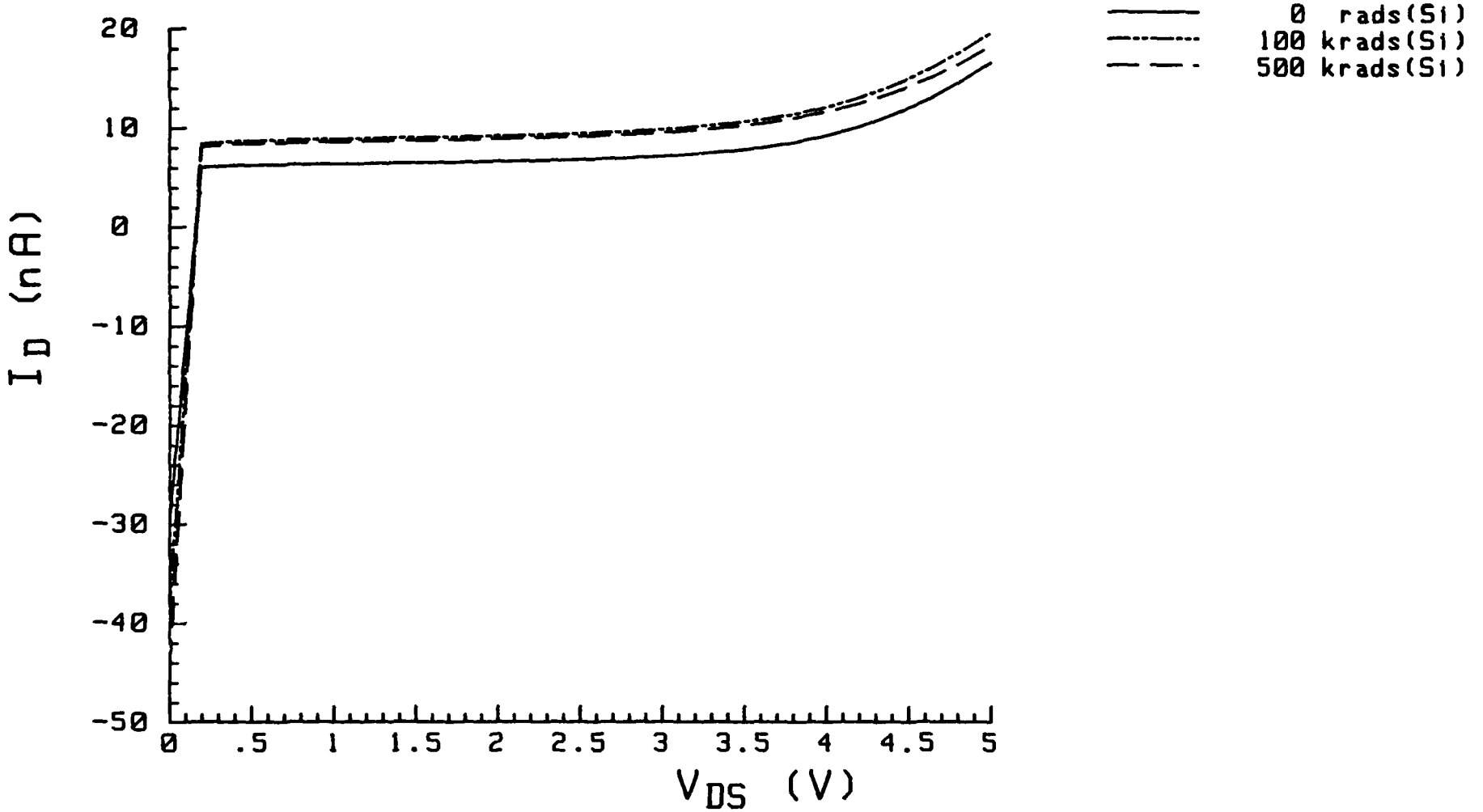


Figure 20.A Total Dose Response of I_D-V_{DS} Characteristics of an H-gate 1.2um n-channel SOI MOSFET with Body Contact (Type B).
V_{BS}=0.6V, V_G=-3V, V_{G1}=-15V
V_{G1}=0V during irradiation

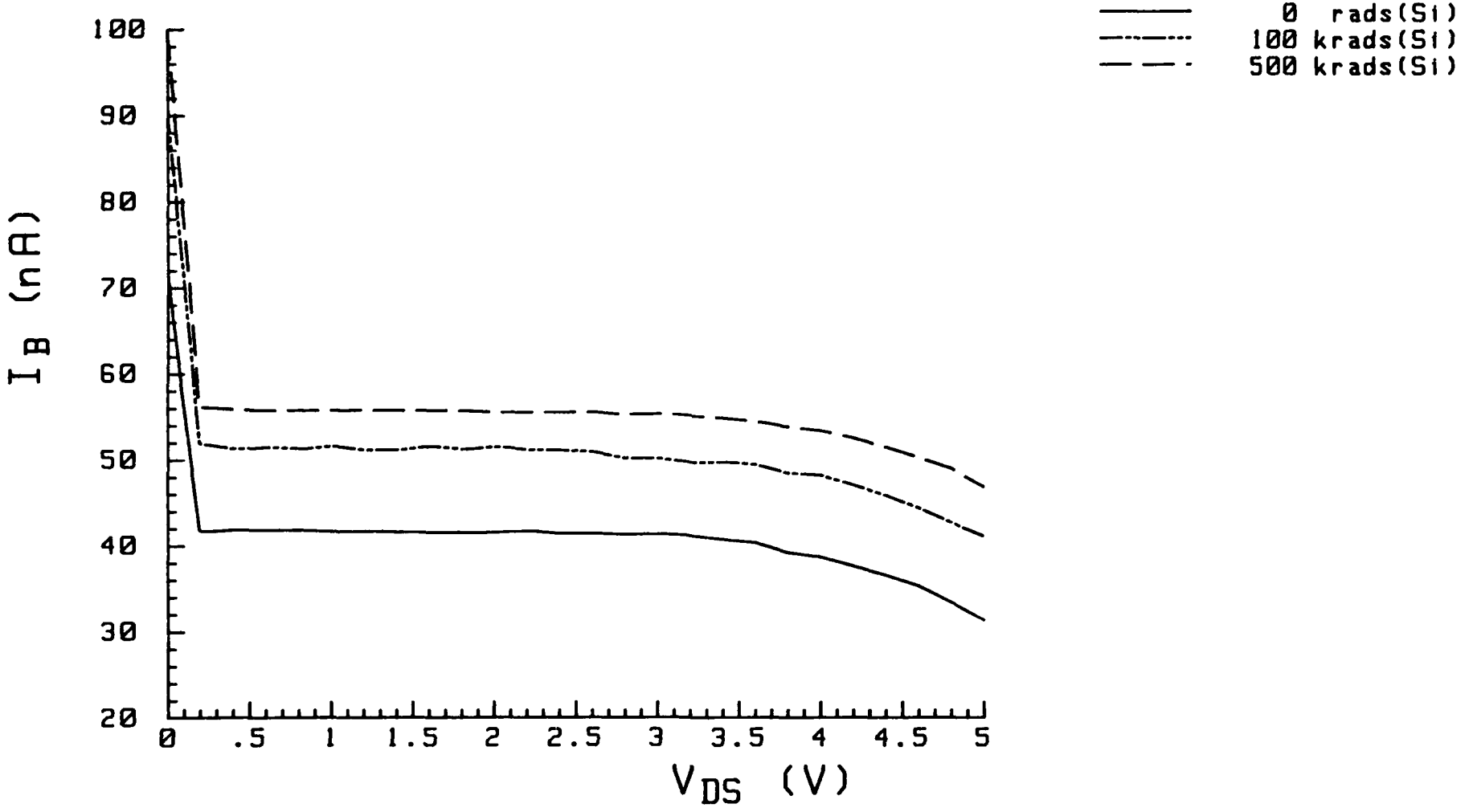


Figure 20.B Total Dose Response of I_B-V_{DS} Characteristics of an H-gate 1.2um n-channel SOI MOSFET with Body Contact (Type B).
V_{BS}=0.6V, V_G=-3V, V_{G1}=-15V
V_{G1}=0V during irradiation

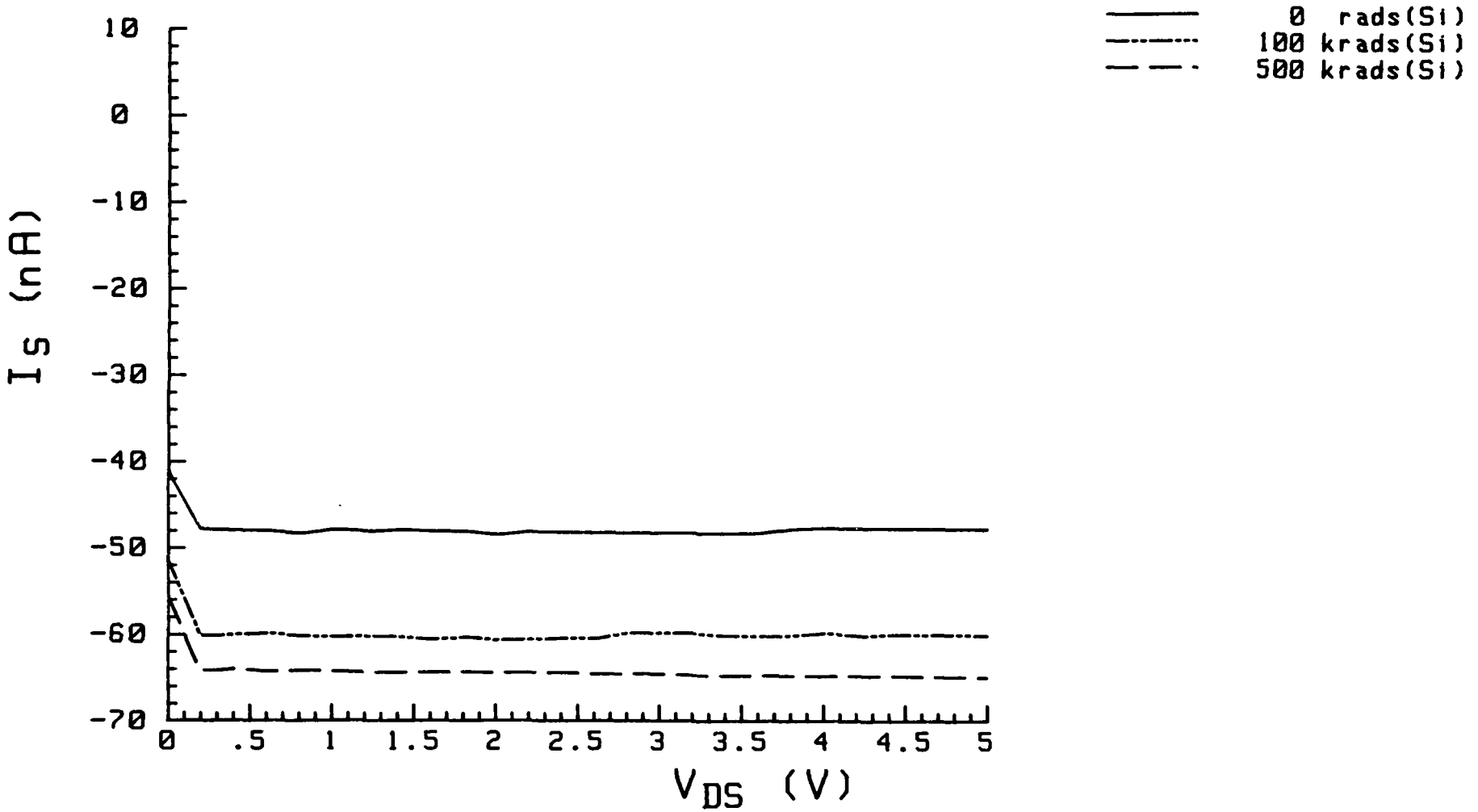


Figure 20.C Total Dose Response of I_S-V_{DS} Characteristics of an H-gate 1.2um n-channel SOI MOSFET with Body Contact (Type B).
V_{BS}=0.6V, V_G=-3V, V_{G1}=-15V
V_{G1}=0V during irradiation

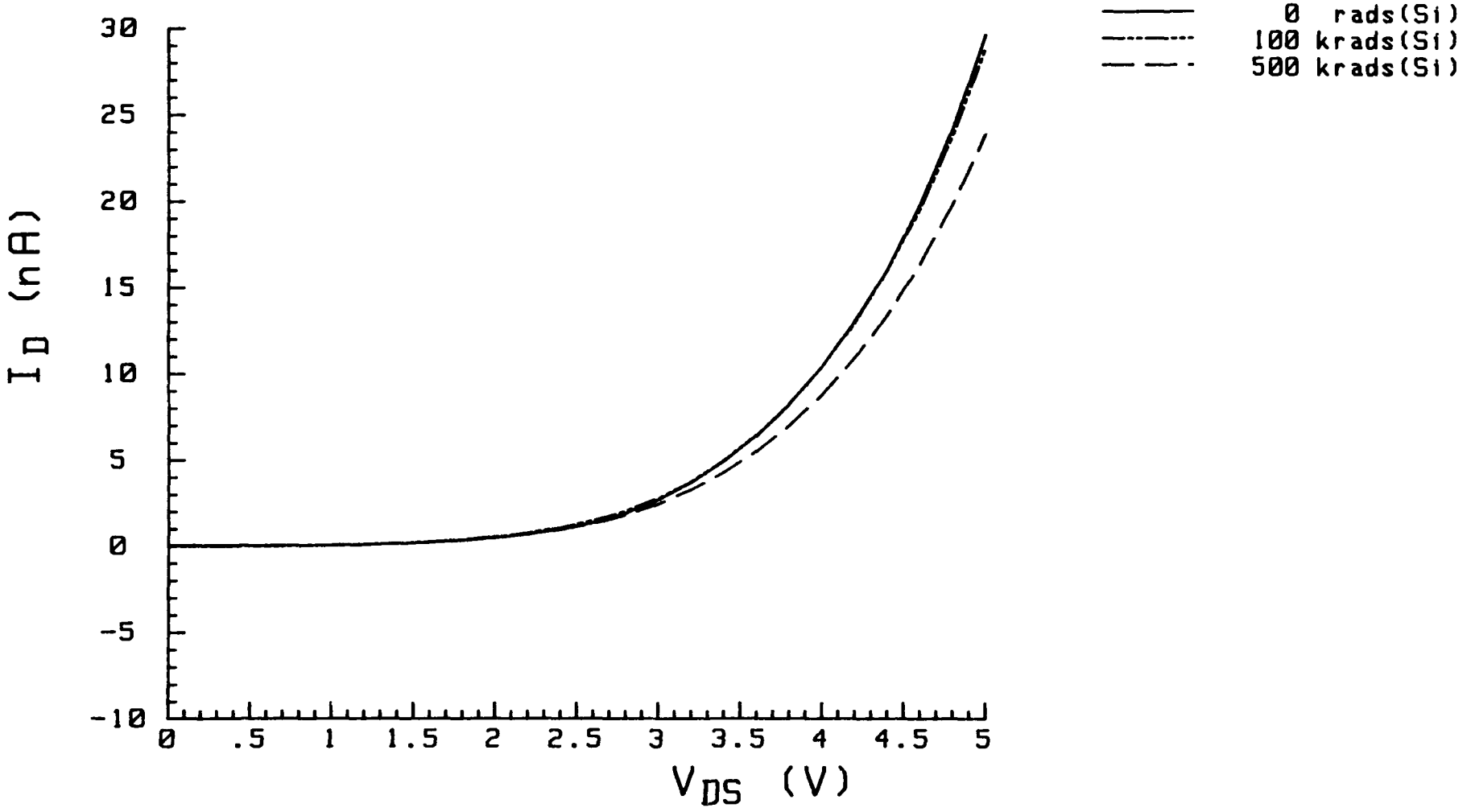
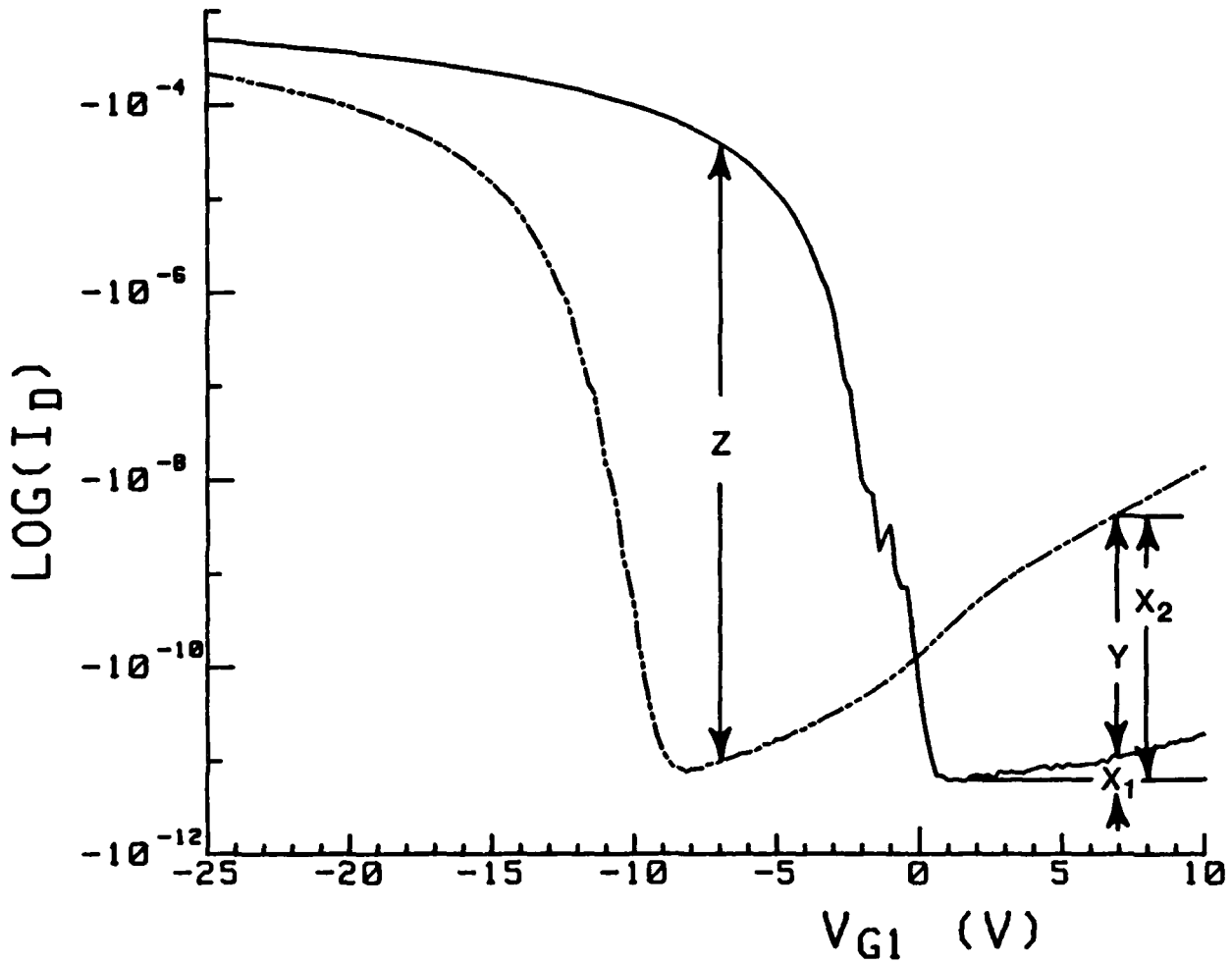


Figure 21. Total Dose Response of I_D-V_{DS} Characteristics of an H-gate 1.2um n-channel SOI MOSFET with Body Contact (Type B).
V_{BS}=-0.6V, V_G=-3V, V_{G1}=-15V
V_{G1}=0V during irradiation



0 rads(Si)
500 krads(Si)

$V_G = 3V$, $V_{DS} = -5V$

Z: BACK-CHANNEL LEAKAGE DUE TO MOSFET ACTION

X_1: SOFT REVERSE LEAKAGE 0 RADS (Si)

X_2: SOFT REVERSE LEAKAGE AT 500 krads (Si)

Y: INCREASED SOFT REVERSE LEAKAGE.

Figure 22. Separation of Leakage Currents for a p-channel Device